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Note 2: A bar by the page number in this page indicates pagination rather than content has changed.

Preface

This manual explains how to operate, handle, and maintain the 2311K/M2312K micro-disk drives.

The information is provided in 10 sections:

SECTION 1 **GENERAL DESCRIPTION OPERATION** SECTION 2 SECTION 3 **INSTALLATION** SECTION 4 THEORY OF OPERATION SECTION 5 TROUBLESHOOTING GUIDE SECTION 6 **MAINTENANCE SPARE PARTS LIST** SECTION 7 **SECTION 8** IC DETAIL SECTION 9 **PARTS LIST SECTION 10 SCHEMATICS**

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Section 1 **General Description**

1. GENERAL DESCRIPTION

1.1 GENERAL DESCRIPTION

1.1.1 General Description

This manual describes the Fujitsu 8-inch rigid disk drives M2311/M2312. These units contain non-removable disks in a sealed module. A rotary actuator using a closed loop servo performs head positioning.

These drives have floppy disk drive dimensions and can be mounted horizontally two drives wide in a 19-inch rack (with 3 pitch) or mounted vertically in a system cabinet.

The contact start/stop (CSS) type heads and media are of the Winchester technology type. These units feature high performance, high reliability and low cost.

The maximum unformatted storage capacities of the M2311 and M2312 units are 48MB and 84MB, respectively.

The M2311 and M2312 utilize the industry standard SMD interface, thereby allowing the drives to be added to an existing disk configuration.

By standardizing on the SMD interface, development time for controllers and software will be substantially reduced. Fixed and variable sector length formats are internally selectable.

To power the drives only DC voltages of +24, +5 and -12 volts are required. This allows for international use. Total nominal power consumption is less than 130 watts.

1.1.2 Features

- (1) High reliability
 - (a) Winchester type technology contact-start/stop (CSS) heads and media are used.
 - (b) Each head has an LSI circuit on its arm to amplify the small signal thereby reducing read errors by increasing the signal to noise ratio.
 - (c) The heads, media and positioning mechanism are sealed in a closed-loop air filtration system.
 - (d) The electrical components located within the sealed disk area are minimized.

(2) Maintainability

No scheduled maintenance is required.

The use of a completely sealed DE, a belt-eliminating built-in DC spindle motor, as well as highly reliable printed circuit assemblies, the necessity of maintenance is greatly reduced.

(3) Compact, Lightweight

This unit can be mounted, two drives across in a standard 19-inch rack. The dimensions are almost floppy disk drive compatible. The weight of the unit is approximately 24 pounds (11 kg). Mounting equipment for the 19-inch rack can be provided as an option.

- (4) Vertical/horizontal Mount Capability
 - These units may be mounted vertically or horizontally within a system cabinet.
- (5) Low accoustical noise level and low vibration allow for installation in an office environment.
- (6) Uses only DC voltages. No internal changes are necessary for changes in frequency or power.

1.2 SPECIFICATIONS

1.2.1 Unit Specifications

The basic specifications of the disk drive are as follows:

Table 1-2-1 Basic Specifications

Model	Specification	Storage capacity
M2311K	B03B-4595-B001A	48.2M bytes
M2312K	B03B-4595-B002A	84.4M bytes

1.2.2 Physical Specifications

Table 1-2-2 Physical Specifications

Item	Conditions	Specifications
Dimension	Height	127mm (5.0")
	Width	216mm (8.5")
	Depth	380mm (15.0")
Weight *		11 kg (24.2 lb)
Temperature	Operating	5°C to 40°C (41°F to 104°F)
	Non-operating	-40°C to 60°C (-40°F to 140°F)
	Gradient	Less than ±15° C/hour
Humidity	Operating	20% to 80% RH
	Non-operating	5% to 95% RH (Non-condensation)
Vibration resistance	Operating	Less than 0.2G (3 to 60 Hz) (2 minutes in both ways x 30-cycle sine wave)
	Non-operating	Less than 0.4G (3 to 60 Hz) (2 minutes in both ways x 30-cycle sine wave)
	Transporting and storing	Less than 3G (non-cyclic)
Altitude	Operating	Less than 3,000m (10,000 feet)
	Non-operating	Less than 12,000m (40,000 feet)
Dust		Less than 0.168 mg/m³ (Stearic acid standard)

^{*} Optional units are excluded.

1.2.3 Power Requirements

The M2311 and 2312K requires +5V, -12V and +24V DC voltages from an optional power supply or system power supply. Each load current required by the drive is shown in Table 1-2-3.

Table 1-2-3 DC Power Requirement

DC Voltage	Load Current (Basic)	Load Current (With Dual Port)
+5V ± 5%	3.5A	4.5A
-12V ± 5%	3.0A	4.0A
+24V ± 10%	3.0A (Effective, type	pical) 6.0Ao-p Maximum

The load currents of +5V DC and -12V DC will be stable even though any operation will be performed within the disk drive, however, the load current of +24V DC will be varied through a power up sequence or DC motor acceleration and/or seek operation.

The +24V DC load current profile during power up sequence is shown in Figure 1-2-1.

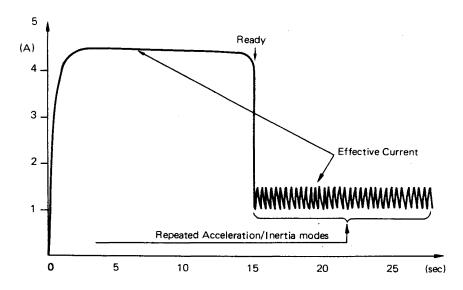


Figure 1-2-1 +24V DC Load Current on Power Up Sequence

The +24 DC load current profile during the repeated acceleration/inertia modes of DC motor and/or seek operation after Ready status is shown in Figure 1-2-2.

Caution: To prevent damage to the power driver (TUZM) PCA and spindle motor, all DC return lines (+5, +24, -12) must be made electrically common at the power supply.

This is already incorporated into the optional Fujitsu power supply.

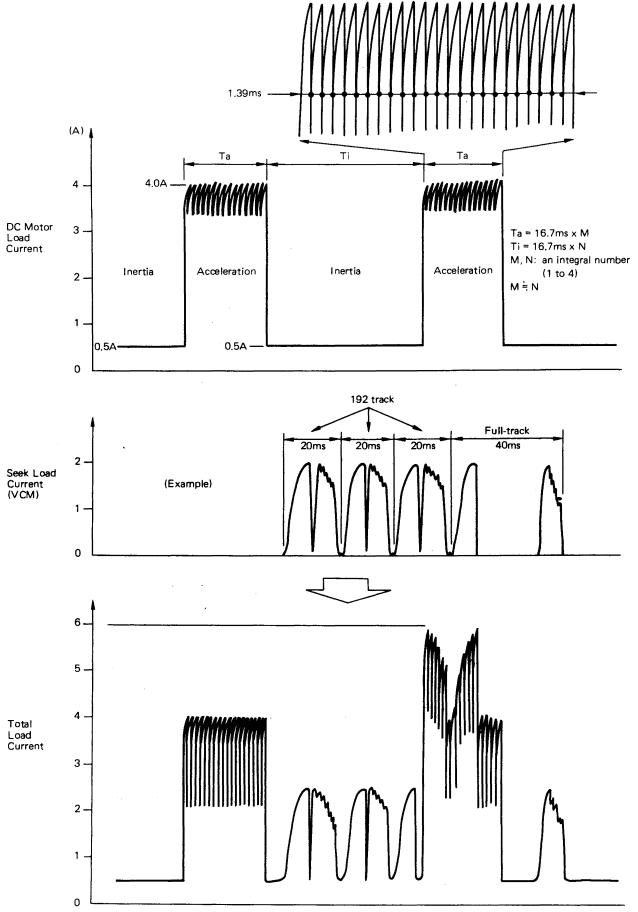


Figure 1-2-2 Total +24V DC Load Current (Ready)

1.2.4 Data Recording SpecificationsData recording specifications are presented in Table 1-2-4.

Table 1-2-4 Data Recording Specifications

	Specifications	
l tem	M2311	M2312
Storage capacity (unformatted)	48,250,880 by tes 84,439,040	
Number of cylinders	589	589
Tracks per cylinder	4	7
Cylinder capacity	81,920 by tes	143,360 by tes
Track capacity	20,480 bytes	
Average rotational latency	8.3 ms	
Positioning time: Track to track	5 ms	
Average	20 ms	
Maximum	40 ms	
Rotational speed	3,600 rpm ± 1%	
Transfer rate	1.229 MB/sec	
Encoding method	MFM	
Interface data	NRZ	
Recording density	9,550 BPI	
Track density	720 TPI	
Start/Stop time	< 20/< 40 sec	
Interface	SMD	
Number of sectors	128 (maximum)	

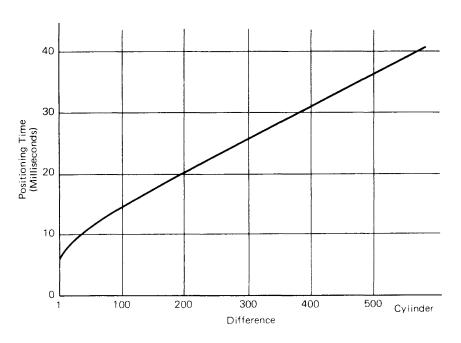


Figure 1-2-3 Positioning Time Profile

1.2.5 Reliability

(1) Mean Time between Failure (MTBF)
The MTBF is defined as follows:

MTBF = Estimated Operating Hours
Number of Equipment Failures

The MTBF shall exceed 10,000 hours (design value). Estimated operating hours should not include any maintenance time. Equipment failures means any stoppage or substandard performance of the equipment because of equipment malfunction, excluding that caused by operator error, cable failure, or other failure not due to the equipment. To establish a meaningful MTBF, operating hours must be greater than 6,000 hours and shall include field performance data from all field sites.

For the purpose of this specification, equipment failures are defined as those failures necessitating repair or replacement on an unscheduled basis.

(2) Mean Time to Repair (MTTR)

The mean time to repair shall not exceed 1.0 hour. It is defined as the time for an adequately trained and competent service technician to diagnose and correct a malfunction.

(3) Preventive Maintenance Time
No scheduled maintenance is required.

(4) Service Life

The M2311/M2312 drive provides a useful life of five (5) years before factory overhaul or replacement is required.

(5) DC Power Loss

Data integrity is assured in the event of a power loss (data is not assured during write operation).

1.2.6 Data Integrity

The following error rates assume that the M2311/2312 is being operated within specification. Errors caused by media defects or equipment failures are excluded.

1.2.6.1 Read Errors

Prior to determination of a read error rate, the data shall have been verified as written correctly and all media defects flagged.

(1) Recoverable Error Rate

A recoverable read error is one which can be read correctly within four retries when reading on track, and should not exceed ten per 10¹¹ bits.

(2) Unrecoverable Error Rate

An unrecoverable read error is one which cannot be read correctly within sixteen retries and should not exceed ten per 10¹⁴ bits.

1.2.6.2 Positioning Error Rate

The positioning error which can be corrected within one retry should not exceed ten per 10^8 seeks.

1.2.6.3 Media Defects

A media defect is defined as a repeative read error that occurs on a properly adjusted drive within specific operating conditions.

Valid data must not be written over known media defects, therefore, sector/track deallocation or skip displacement techniques must be utilized.

(1) Media Defect Characteristics

a) The maximum number of defects per drive is as follows:

M2311K (48MB): 56 M2312K (84MB): 98

b) The maximum number of defective tracks per drive is as follows:

M2311K (48MB): 8 M2312K (84MB): 14 A defective track is defined as a track having any of the following:

- 1. Two or three defects.
- 2. Defective logging areas

Note: No track shall have more than three defects.

- (2) Media defect free areas are defined as follows:
 - 1. Cylinder 0, Head 0 through 2
 - 2. Any error in logging area to extent defined in the Media Defect Format

1.2.6.4 Media Defect Information

All MDD will have a Media Defect List which will list the following information.

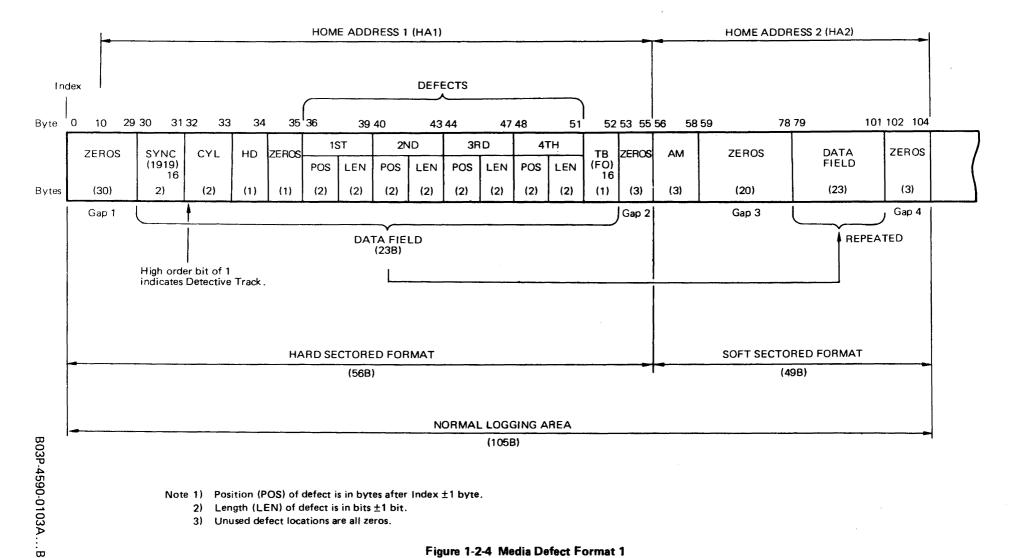
- 1. Cylinder Address
- 2. Head Address
- 3. Position (bytes from Index ±1 byte)
- 4. Length (bits ± 1 bit)

The above information will be listed by hexadecimal code. The maximum media defect length at a defect is 64 bytes (512 bits).

1.2.6.5 Media Defect Format

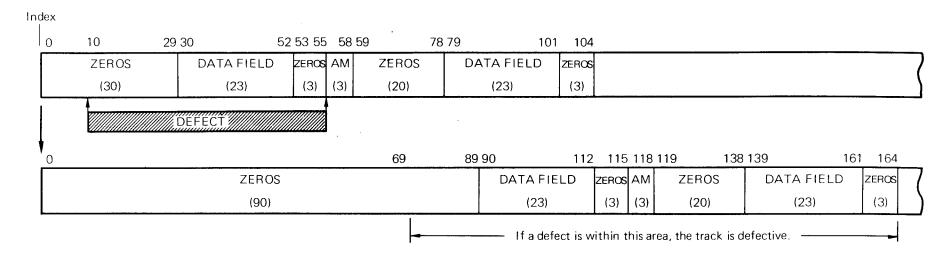
The MDDs will be formatted at the factory with standard Media Defect Format. The Media Defect Format is divided into two parts. The first part is a hard-sectored format and is normally included in the first 56 bytes following Index signal. The second part is a soft-sectored format and is normally included in the next 49 bytes following Index signal as shown in Figure 1-2-4 Format 1. The format rules are as follows:

- 1. A track which has more than one defect is defined and flagged as a defective track. The first four media defects are logged.
- 2. If the beginning of a defect is located between Byte 10 to Byte 55 (HA1) after Index, 60 bytes of zeros are added to gap 1 (90 bytes total). In this case, if any part of a defect is located between Byte 69 and Byte 164 (HAR1' and HA2'), the track is flagged as defective. Refer to Figure 1-2-5 Format 2.
- 3. If the beginning of a defect is located between Byte 56 and Byte 104 (HA2) after Index, 60 bytes of zeros are added before Address Mark (AM). In this case, if any of a defect is located between Byte 116 and Byte 164 (HAR"), the track is flagged as defective. Refer to Figure 1-2-5 Formats.
- 4. If the track is defined as a defective track according to above-mentioned Rule 1, 2 or 3, the high order bit of the first cylinder address byte is set to 1. Remaining information may or may not be valid.



- Note 1) Position (POS) of defect is in bytes after Index ±1 byte.
 - 2) Length (LEN) of defect is in bits ±1 bit.
 - 3) Unused defect locations are all zeros.

Figure 1-2-4 Media Defect Format 1



Format 2

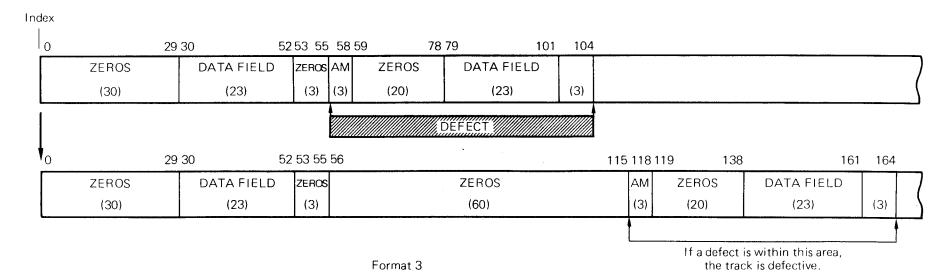
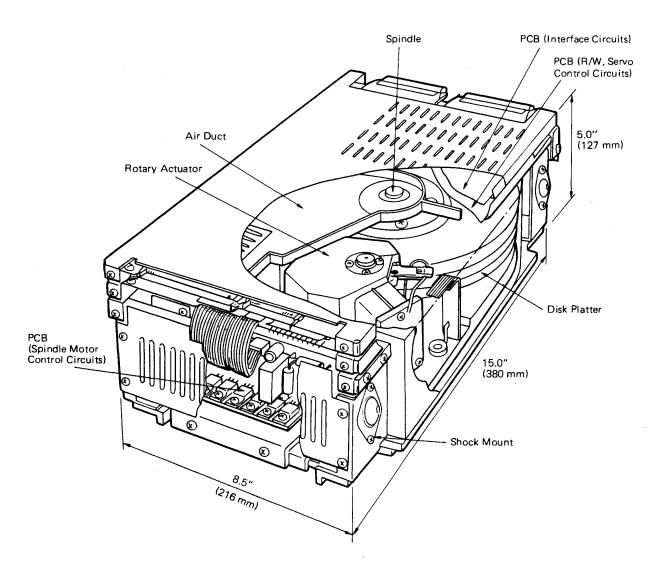


Figure 1-2-5 Skip Displaced Format

1.3 CONFIGURATION

1.3.1 Fundamental Unit Configuration

Figure 1-3-1 shows the fundamental configuration of the unit; Figure 1-3-2 shows the block diagram.



Note: The M2311 has three disks (four R/W heads) in the DE, the M2312 has four disks (seven R/W heads) in the DE.

Figure 1-3-1 Standard Configuration of the M231XK

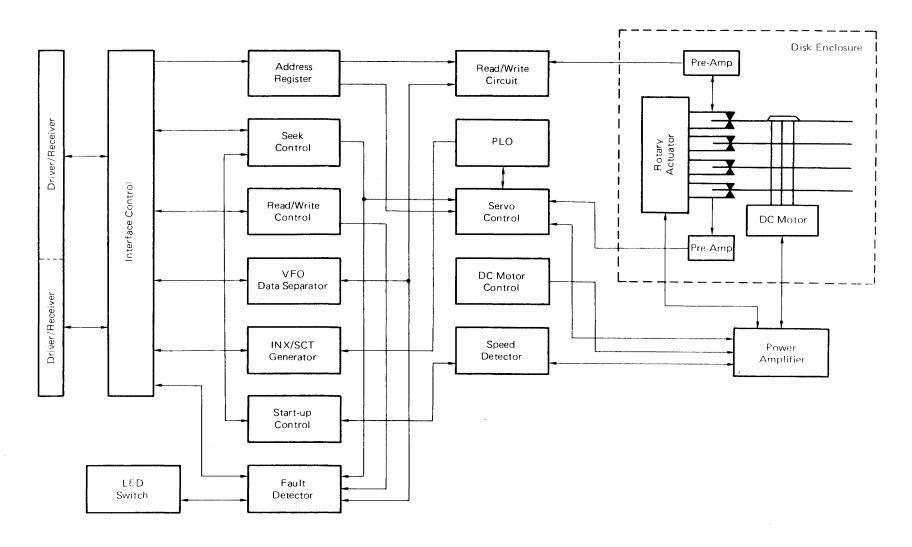


Figure 1-3-2 Block Diagram

1.3.2 Options

Optional items are presented in Table 1-3-1.

Table 1-3-1 Options

Item No.	Component name	Specification (Drawing No.)	Remarks
1-1	Fan unit	B03B-4590-E002A	100/115/120V AC; 50/60 Hz
1-2	Fan unit	B03B-4590-E003A	220/240V AC; 60 Hz
2-1	Power supply unit	B14L-5105-0100A	 100/115/120/220/240V AC. With connectors for feeding power to fan units and dual channel printed board unit.
3-1	Cable	B660-1065-T006A	Interface cable (A) 60P flat cable
3-2	Cable	B660-1065-T008A	Interface cable (B) 26P flat cable
3-3	Cable	B660-1865-T020A	Interface cable (A) for 2 units daisy chain
3-4	Cable	B660-1865-T030A	Interface cable (A) for 3 units daisy chain
3-5	Cable	B660-1865-T040A	Interface cable (A) for 4 units daisy chain
3-6	Cable	B660-1865-T050A	Interface cable (A) for 5 units daisy chain
3-7	Cable	B660-1865-T060A	Interface cable (A) for 6 daisy chain
3-8	Cable	B660-1865-T070A	Interface cable (A) for 7 units daisy chain
3 -9	Cable	B660-1865-T080A	Interface cable (A) for 8 units daisy chain
4-1	Panel unit	B03B-4590-E501A	Flat key type control panel board
5-1	Mounting tray	B030-4590-T500A	For mounting two units of 19-inch rack with 3 pitches (inside frame)
5-2	Mounting tray	B030-4590-T501A	For mounting two units of 19-inch rack with 3 pitches (inside frame), and the front panel has the windows for operating the panel unit.
5-3	Brackets	B030-4590-T550A	 For mounting two units of 19-inch rack with 3 pitches (outside frame) Length setting pitch: 586 mm — 686 mm
6-1	Dual Channel	B03B-4590-E401A	To be mounted on optional PSU.
6-2	Dual Channel	B03B-4590-E402A	To be mounted on drive unit.
7-1	Power cable	B660-0625-T327A	Drive unit — power supply unit connecting
8-1	Cable	B660-0625-T328A	E002A fan unit — power supply unit connecting
8-2	Cable	B660-0625-T355A	E003A fan unit connecting
9-1	Cable	B660-1995-T003A	E501A panel unit — drive unit connecting
10-1	Cable	B660-0625-T329A	Dual channel PCB assy. — Power supply unit connecting

Note: Items in the above table are optional and not fundamental components of this unit. These items must be ordered separately conforming to the above specifications as occasion demands.

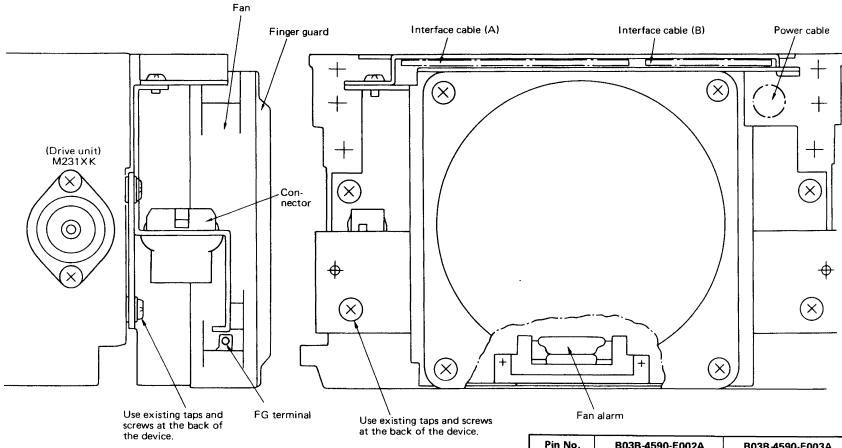
1.3.2.1 Fan Unit

The M2311K/M2312K requires some means of cooling, since there is no internal blower motor. For this purpose, optional fan units is available. The fan unit is available in the event that adequate cooling is not provided within the mounting cabinet. This fan unit is directly mountable onto the hind of the device, and be mounted also at the field by using the existing screws and taps.

The fan unit may be ordered in any of the following voltage ratings: 100/115/125V AC or 220/240V AC. When the input power of the fan unit is supplied from the optional power supply unit, the fan unit must be ordered the type for 100/115/120V AC (B03B-4590-E002A) regardless of system AC voltage.

The Figure 1-3-3 shows the mounting status, I/O terminals, etc., of the fan unit.

1-13



*1: The overall length after mounting the fan unit is 430 mm (380 mm + 50 mm).

*2: Fan Alarm Specification

Type of contact point: Normal open Contact capacity: 0.5A DC Max.

200V DC Max.

* However: i (A) \times E (V) \leq 10W DC

Rated power (Heater): 4.2W (at 100V AC)

Response time: Circuit: 5-300 sec. as follows

Figure 1-3-3 Fan Unit

Pin No.	B03B-4590-E002A	B03B-4590-E003A
1	100/115/120V AC	220/240V AC
2	100/115/120V AC	
3	FG	FG
4		220/240V AC
5	ALARM (*2)	ALARM (*2)
6	ALARM (*2)	ALARM (*2)

Fan Unit Connector Part Number Connector AMP 1-480704-0 Contact AMP 350550-1

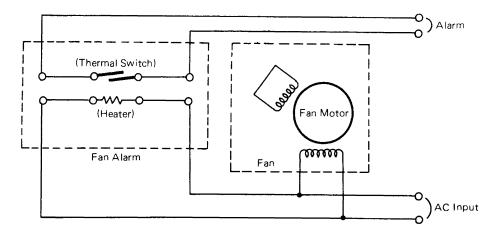


Figure 1-3-4 Optional Fan Unit Alarm

1.3.2.2 Power Supply Unit

A power supply unit may either be mounted horizontally behind the disk drive or may be mounted vertically. Figure 1-3-5 shows the details of I/O terminals and the external dimensions of the power supply unit.

Specification: B14L-5105-0100A

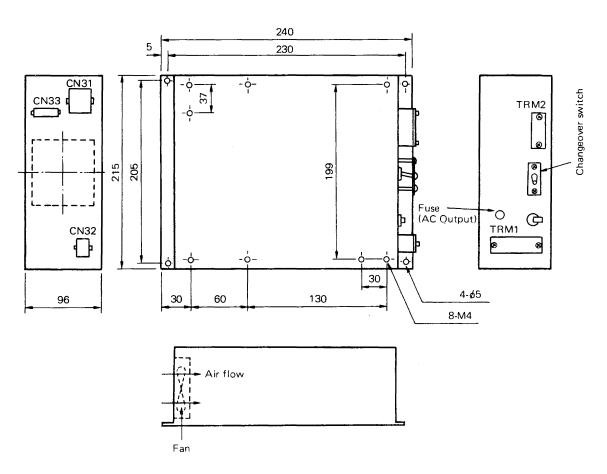


Figure 1-3-5 Power Supply Unit

TRM1: AC power input and alarm sending.

TRM2: FG-SG coupling terminal. (Normally open)

CN31: Drive unit power feeding connector

(for cable B660-0625-T327A (Option))

CN32: Fan unit power feeding connector

(for cable B660-0625-T328A/T355A (Option))

CN33: Dual channel PCB unit power feeding connector

(for cable B660-0625-T329A (Option)

AC input voltage selection from 100/115/120V AC to 220/240V AC is switched selectable.

Also, regardless of AC input voltage, AC output voltage from CN2 (fan unit power supplying connector is kept $115V + 15\% \\ -24\%$ AC.

Therefore when using the option power supply only the 115V AC fan is required.

1.3.2.3 Panel Unit

The panel unit includes function lights which indicate power on, ready, write protect, check, and also includes a write protect switch and a check clear switch.

Figure 1-3-6 shows the mounting dimensions and mounting status of panel unit B03B-4590-E501A.

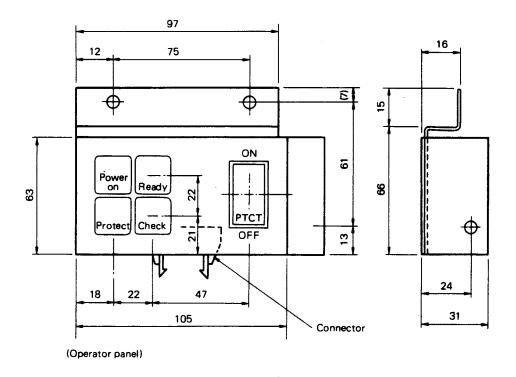


Figure 1-3-6 Panel Unit

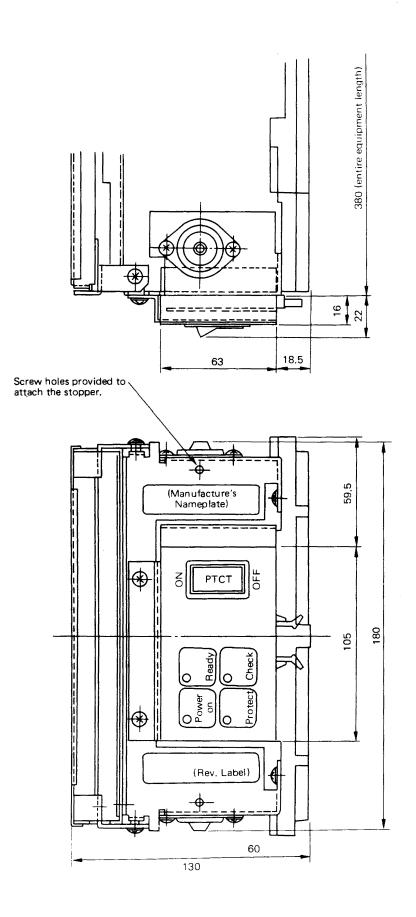


Figure 1-3-7 Mounting Dimensions of Panel Unit

1.3.2.4 19" Rack Mount Installation

Mounting-tray with brackets is possible to install two drives, side by side in a 19" rack, three pitches. It can also accommodate the optional fan units and/or power supply units for each of the two drives.

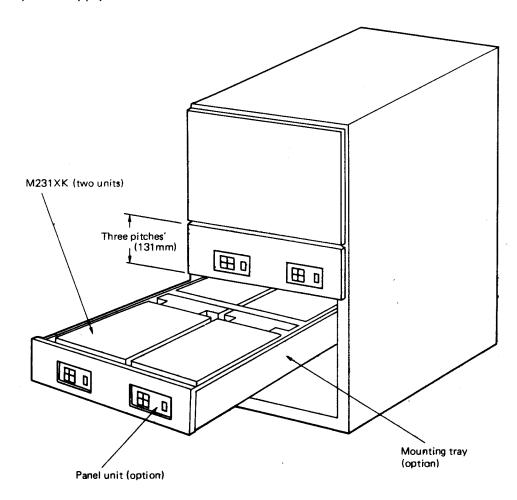
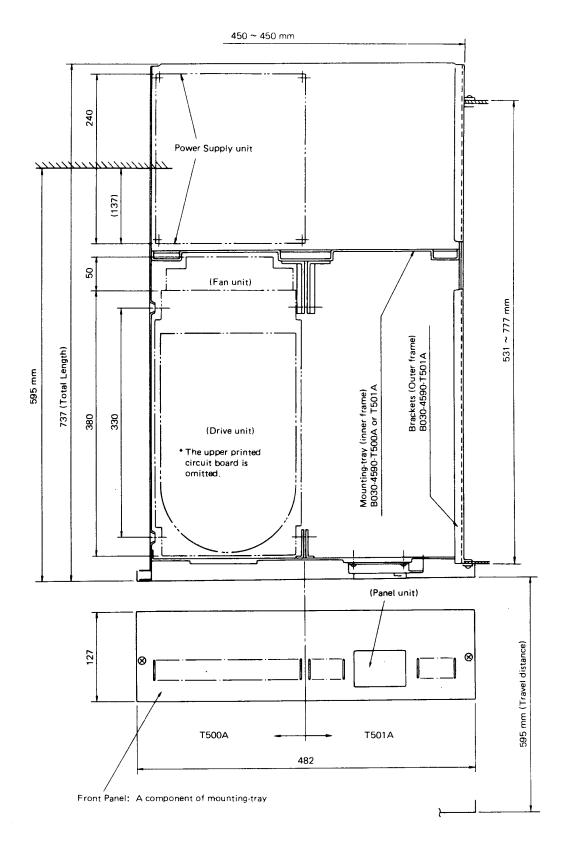


Figure 1-3-8 19" Rack Mount Installation

Mounting-tray (inner frame) guided by brackets (outer frame) can be drawn out forward. (Travel distance is approximately 23.4").

19" rack mounting method is illustrated in Figure 1-3-8. And Figure 1-3-9 shows the appearance where the units are mounted in mounting-tray and brackets.



Note: Mounting-tray (T500A) cannot accommodate the drive unit with Panel unit. In that case, T501A-type must be specified.

Figure 1-3-9 Mounting-Tray and Brackets

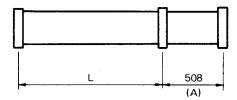
1.3.2.5 Cables

The interface cable (A) is up to 30m long (to the drive unit at the final step in case of daisy chain mode). The length of the cable can be specified in every 20 inches (508 mm).

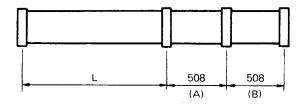
The interface cable (B) is up to 15m long. The length of this cable can be specified in every 500mm.

The (A) cables for daisy-chain connection shown at items 3-3 to 3-9 in Table 1-3-1 are of the forms as shown in Figure 1-3-10. Cable length "L" (specifiable by "#L") refers to the corresponding sections of the following drawings:

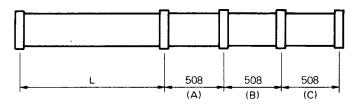
· For B660-1865-T020A



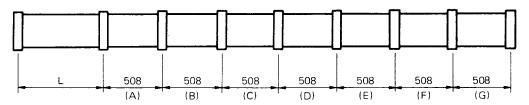
· For B660-1865-T030A



For B660-1865-T040A



· For B660-1865-T080A



The connectors at both ends are of close end, while the intermediate connectors are of through end.

Figure 1-3-10 A-Cables for Daisy-Chain

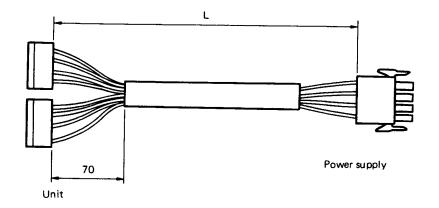


Figure 1-3-11 Power Cable B660-0625-T327A

How to specify cable lengths

(For 3.5m: Example 1)

 $\frac{B660-1065-T008A}{\text{Cable specification}} \quad \frac{\#\text{L3R503}}{3.5 \times 10^3 \, \text{(mm)}}$

(For 50cm: Example 2)

 $\frac{\text{B660-0625-T327A}}{\text{Cable specification}} \quad \frac{\text{\#L500R0}}{\text{500} \times 10^{0} \text{ (mm)}}$

The lengths of cables at Items 7, 8, 9 and 10 in Table 1-3-1 must also be specified.

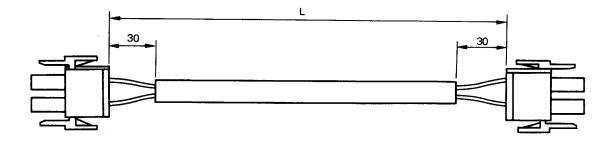


Figure 1-3-12 Cable B660-0625-T328A, T355A (Fan unit — Power supply unit)

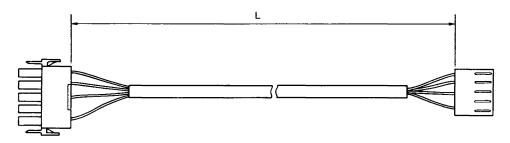


Figure 1-3-13 Cable B660-0625-T329A (Dual Channel PCB assy. — Power supply unit)

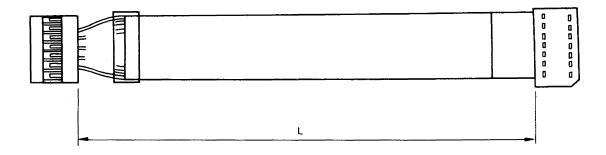


Figure 1-3-14 Cable B660-1995-T003A (E501A Panel unit — Drive unit connecting)

The length of this cable can be specified in every 60 mm. (Minimum length is 90 mm.)

Operator Panel Connection

The CNAM PCB allows for connection of an optional control panel. At location A5 on this PCB, there is a 14 pin DIP socket for the control panel connection. Following is pin-out for this DIP socket.

PIN NUMBER	SIGNAL MNEMONIC	DEFINITION
1	+5V	+5 Volt
2	*FPTK	File Protect Switch
3	*CKCLR	Check Clear Switch
4	*LRDY	Ready LED
5	0V	Signal Ground
6	*LUSLD	Unit Selected LED
7	0V	Signal Ground
8	0V	Signal Ground
9	*PWRDY	Power Ready LED
10	*LFPT	File Protect LED
11	*LDYCK	Device Check LED
12	0V	Signal Ground
13	0V	Signal Ground
14	+5V	+5 Volt

[&]quot;*" Indicates a low active signal.

1.3.2.6 Dual Channel PCB Assembly

This unit is provided with the dual channel option to add the crosscall function, and it is possible to be mounted on the unit or the power supply.

Drive's high are:

- · In case of mounting on the unit; 154 mm
- In case of mounting on the power supply; It is possible to be mounted in the 19-inch rack with 3-pitch by using the optional power supply (B030-4590-T500A or T501A), the mounting-tray (B030-4590-T500A or T501A), and the bracket assembly.

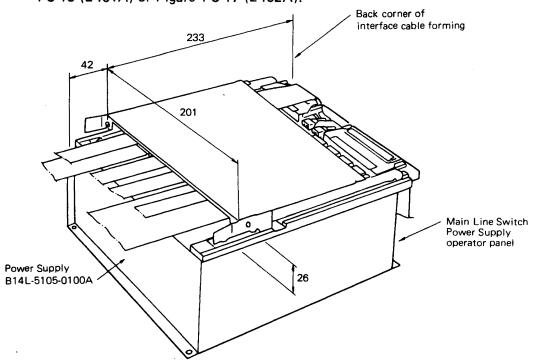
The specifications and the rating of dual channel option are shown in Table 1-3-2.

Table 1-3-2 Dual Channel Option

Specifications	B03B-4590-E401A	B03B-4590-E402A	
Mounting location	On the power supply	On the unit	

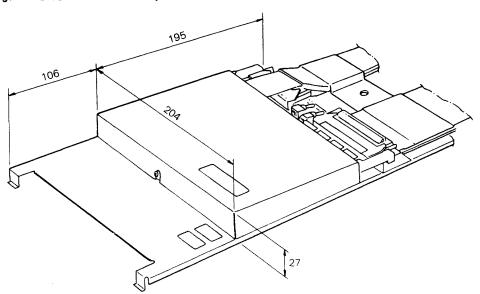
Note: The dual channel option is connected with optional power supply by using the connecting cable. (See Item 1.3.2.5)

Dimensions after mounting of Dual channel PCB Assembly are shown in Figure 1-3-15 (E401A) or Figure 1-3-17 (E402A).



Note: In case of mounting on the power supply, fix Brackets with screws on the power supply.

Figure 1-3-15 Dual Channel Option (E401A)



Note: In case of mounting on the unit, change the usual unit cover to the cover for this option.

Figure 1-3-16 Dual Channel Option (E402A)

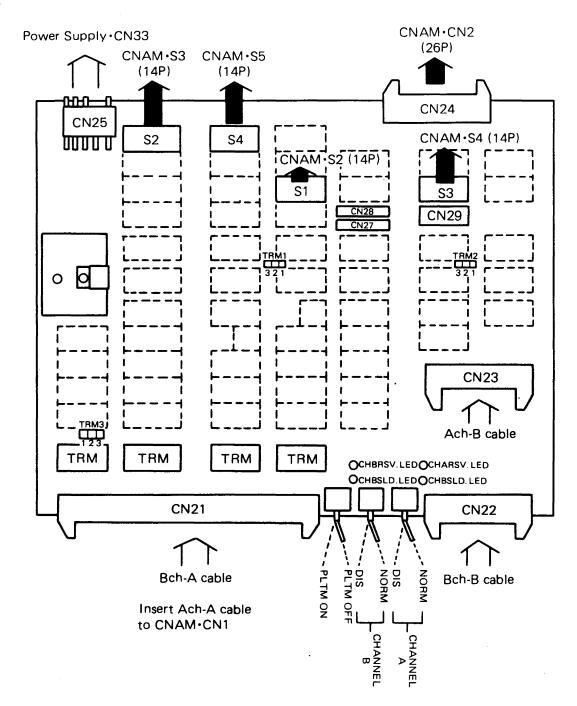


Figure 1-3-17 Dual Channel PCB Assembly Connector Location

Section 2
Operation

2. OPERATION

2.1 GENERAL DESCRIPTION

Two M231X Micro Disk Drive can be horizontally mounted in a 19 inch rack with optional mounts hardware. The M231X may also be built into a system cabinet and mounted horizontally or vertically. A mounting tray (with slide rails) is available.

The CNAM Printed-Circuit-Board Assembly in the M231X Micro Disk Drive is equipped with Maintenance Aid LED's and File Protect switch.

Powering up/down and the functions of the internal installed indicators (LED) and switches will be described in this section. The functions of the LED's and switches on the optional operator panel will also be described.

2.2 POWERING UP/DOWN

The M231X Micro Disk Drive is not equipped with a power ON/OFF switch. Powering up/down of the M231XK's typically performed by a powering up/down of the system.

When the disk unit is equipped with an optional power supply, powering up/down may be performed by turning the power switch ON and OFF at the power supply.

2.3 CONTROL AND INDICATORS

2.3.1 Operator Panel (option)

The functions of the LED's and switches or optional operator panel (front panel) is described below.

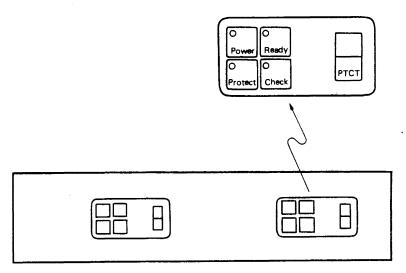


Fig. 2-3-1 Operator Panel (Optional)

(1) Power indicator: Red

This LED lights when the power is turned on.

(2) Ready indicator: Red

This LED indicates the initial seek has performed or indicates the termination of a Seek or RTZ operation.

(3) Check indicator: Red

This LED indicates any fault condition.

(4) Protect indicator: Red

This LED indicates that writing is inhibited.

(5) Protect (PTCT) switch: White

This key inhibites the write operation.

(6) Check clear switch: Gray (flat key)
This key resets a Device Check status.

2.3.2 PCB Assembly

2.3.2.1 CNAM PCB Assembly

The unit contains fault display indicator (LED's) and File-protect switch as shown in Figure 2-3-2. These are location on CNAM PCB.

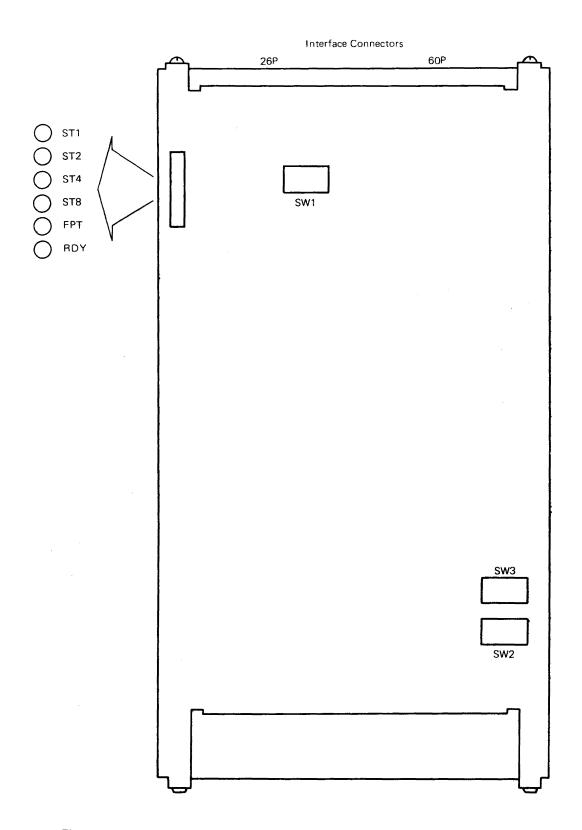


Figure 2-3-2 Fault Display Location on CNAM PCB

- (1) FPT (File Protect) switch: SW1 Key 7
 This switch inhibits the write operation. When an optional panel is installed on the drive, the switch should be in the OFF position.
- (2) RDY (Ready) indicator: Green
 This RDY LED indicates that the initial seek has been performed or indicates the termination of a Seek or RTZ operation.
- (3) FPT (File Protect) indicator: Red
 This LED indicates that writing is inhibited.
- (4) ST1 to ST8 (Status 1 to 8) LEDs: Red Fifteen fault statuses are visible by binary code as shown in Table 2-3-1.

Table 2-3-1 Fault Indicator

Status Bit		Code	Fault Status			
ST8	ST4	ST2	ST1	(Hex)	Fault Description	
0	0	0	1	1	DC motor failure (DMFL)	indicates spindle motor failure.
0	0	1	0	2	VCM over heat (VCMHT)	indicate VCM over-heating.
0	0	1	1	3	Initial seek time out (INTMOT)	indicates initial seek has terminated with time-out.
0	1	0	0	4	Control check 1 (CTCK1)	indicates that a Read/Write command was issued during busy status.
0	1	0	1	5	Control check 2 (CTCK2)	indicates that write gate was issued during a fault condition.
0	1	1	0	6	Read/write check 1 (RWCK1)	indicates that write gate was issued during off-track.
0	1	1	1	7	Read/write check 2 (RWCK2)	indicates that write current did not flow to the head during a Write operation.
1	0	0	0	8	Read/write check 3 (RWCK3)	indicates that write gate was issued during File- Protected status.
1	0	0	1	9	Read/write check 4 (RWCK4)	indicates that write gate was issued during a multi- head-selected status.
1	0	1	0	Α	Time-out (TMOT)	indicates that seek or RTZ sequence was not terminated within 500 ms.
1	0	1	1	В	Seek guard band (SEKGB)	indicates that a guard band was detected during a direct seek operation.
1	1	0	0	С	Linear mode guard band (LNMGB)	indicates that a guard band was detected during a linear mode.
1	1	0	1	D	RTZ outer guard band (RTOGB)	indicates that an outer guard band was detected during an RTZ operation.
1	1	1	0	E	Over-shoot check (OVSHT)	indicates that the head overshoot the new cylinder address during settling time.
1	1	1	1	F	Illegal cylinder check (ILCYL)	indicates that an illegal cylinder address (>588) was issued by the controller.

2.3.2.2 CMZM PCB Assembly

The CMZM PCB assembly is shown in Figure 2-3-3.

Three LEDs are located on the CMZM PCB assembly as follows:

ACDM (Orange): This LED indicates that accelerate Mode in DC motor control

is activated. The LED comes on at power on and stays on continuously until the spindle has reached its nominal rotational value of 3600 RPMs, $\pm 2\%$, (Approx. 20 sec). At this point the DC motor control changes to inertia mode for approximately 67 msec, and the LED goes out. As the spindle speed decreases to within 2% of 3600 RPMs, the DC motor control again activates accelerate mode for approxi-

mately 33 msec, and the LED comes on.

SPGD (Orange): This LED indicates that the spindle speed is within ±6% of

nominal rotational speed. This LED will not come on until

approximately 20 seconds after power on.

PWRDY (Green): This LED indicates that +5V, -12V, +24V and internal +12V

are within the nominal voltage.

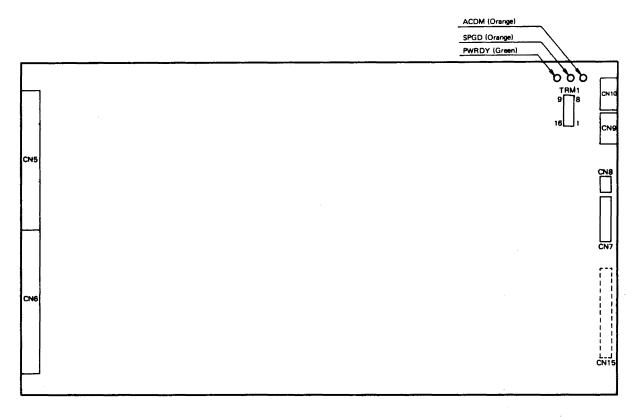


Figure 2-3-3 CMZM PCB Assembly

2.4 Dual Channel PCB Assembly (Option)

Dual channel PCB assembly is shown in Figure 2-5-1.

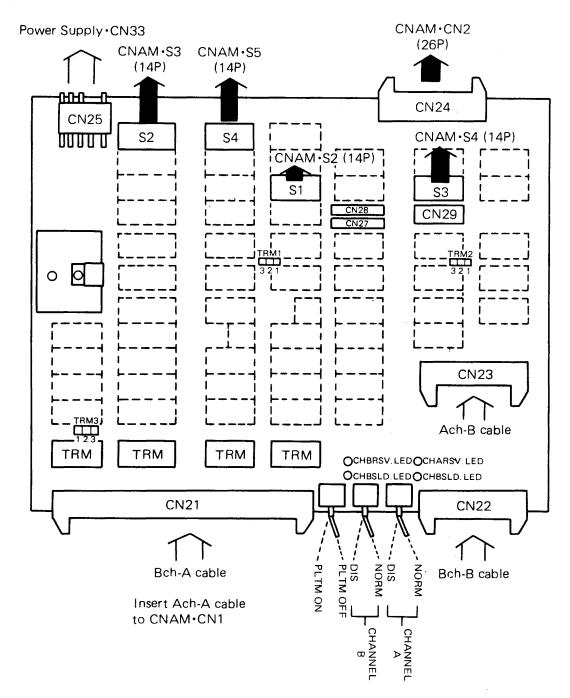


Figure 2-4-1 Dual Channel PCB Assembly

- (1) CHASLD LED (green)
 Indicates that this unit is Selected by the Channel-A controller.
- (2) CHARSV LED (orange)
 Indicates that this unit is Reserved by the Channel-A controller.
- (3) CHBSLD LED (green)
 Indicates that this unit is Selected by the Channel-B controller.
- (4) CHBRSV LED (orange)
 Indicates that this unit is Reserved by the Channel-B controller.

B03P-4590-0103A...B 2-5

(5) CH-A Switch DIS (Disable A): Disconnects the unit from the Channel-A controller and disables it from sending and receiving all interface signals from

Channel A.

NORM (Normal A): Connects the unit to the Channel-A controller and enables it to send and receive interface signals.

(6) CH-B Switch DIS (Disable B): Disconnects the unit from the Channel-B controller and disables it from sending and receiving all interface signals from

Channel B.

NORM (Normal B): Connects the unit to the Channel-B controller and enables it to send and receive interface signals.

(7) RLTM Switch

RLTM ON:

When in "Release Timer On", Reserved and Priority Select are

released 500 ms (nominal) after the unit is deselected.

Note: Reserved and Priority Select can also be released by

the Release Command (TAG 3, BUS 9).

RLTM OFF:

When in "Release Timer Off", the Reserved condition is released from the controller by the Release Command (TAG 3.

BUS 9).

2.5 POWER SUPPLY

The optional power supply may be provided with the M231XK. The front view of the power supply is shown in Figure 2-5-1.

2.5.1 Main Line Switch

This switch controls application of site AC power to the power supply. Turning on the switch applies power to an optional fan unit and DC Power to the disk drive.

2.5.2 Indicators (LEDs)

(1) Power On LED

The Power On LED indicates that AC input is applied to the power supply.

(2) Power Alarm LED

The power alarm indicates the following malfunction has occurred on the power supply:

·+5 VDC: Over-current, Over-voltage and Non-voltage

· - 12 VDC: Over-current and Non-voltage

•+24 VDC: Over-current and Non-voltage

· Over heat within the power supply

· AC Output to the fan: Over-current

2.5.3 Device Alarm

The Device Alarm indicates that the thermal switch has be closed on an optional fan.

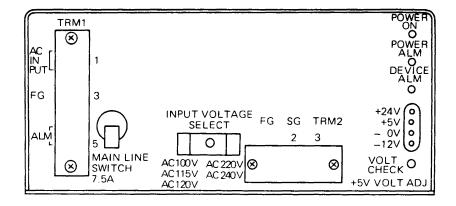


Figure 2-5-1 Front View of Power Supply

Section 3 **Installation**

3. INSTALLATION

3.1 GENERAL DESCRIPTION

This section describes unpacking, installation, and cabling of the M231XK when shipped separately, and shipping precautions when the unit is delivered as a system.

3.2 UNPACKING

The M231XK is wrapped in a polyethylene bag, surrounded cushions, and packed in a carton. An exterior view of the carton is shown in Figure 3-2-1 and Figure 3-2-2.

- (1) Store and open the carton on a flat surface, ensure that the top of the box, indicated by a "This Side Up" signs, is oriented correctly.
 - Note: Don't store on the disk drive upside-down position.
- (2) Take out the top cushion and its partition.
- (3) Pull the M231XK out of the box by grasping its base.

 Move the unit slowly and carefully, to prevent unnecessary shock.
- (4) Take out the lower partition and pull out the optional units, cables, etc.
- (5) Store packing material for possible future use.

Note: When the difference in the storage (or shipping) environment and the unpacking environment exceeds 20°C (36°F), the carton should be allowed to stand at the unpacking site for more than 3 hours prior to unpacking to avoid condensation.

Caution: When unpacking, don't place the M231XK on a bare floor directly to avoid handling damage due to shocks. Place it on a suitable cushioning materials.

3.3 VISUAL INSPECTION

After unpacking, check the following.

- (1) There should be no cracks, rust or other damage that mars appearance and integrity.
- (2) All parts should be firmly fixed, there should be no loose screws, etc.
- (3) The prescribed transportation lock (lock for transportation) should be intact, with no abnormalities.
- (4) The attachments and options should be as ordered.

3.4 INSTALLATION

This unit may be mounted in a 19-inch rack or built into a system cabinet. If mounting the M231XK in a standard, 19-inch rack, the mounting tray and its brackets are provided (as options). When the M231XK is built into a system cabinet, it can be mounted horizontally or vertically.

3.4.1 Mounting Dimensions

Figure 3-4-1 shows the M231 XK dimensions and the structure of its frame.

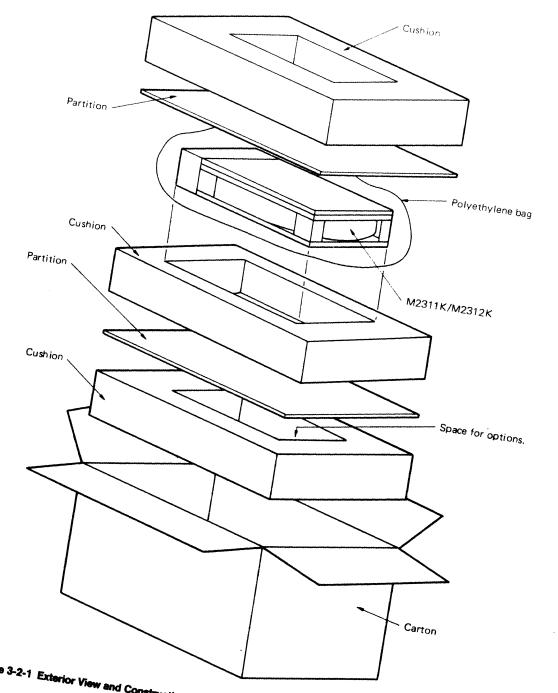
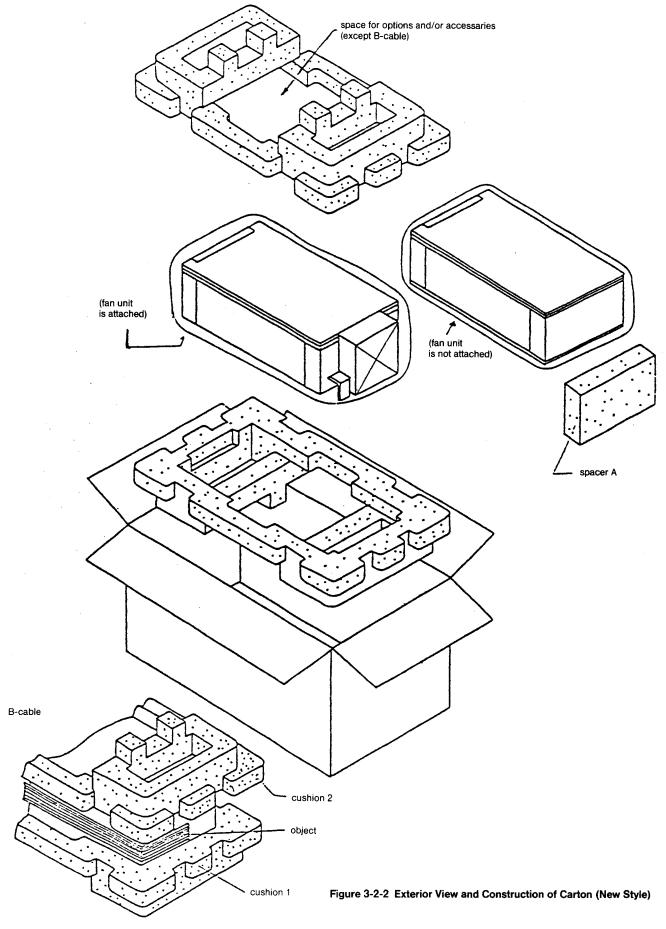


Figure 3-2-1 Exterior View and Construction of Carton (Old Style)



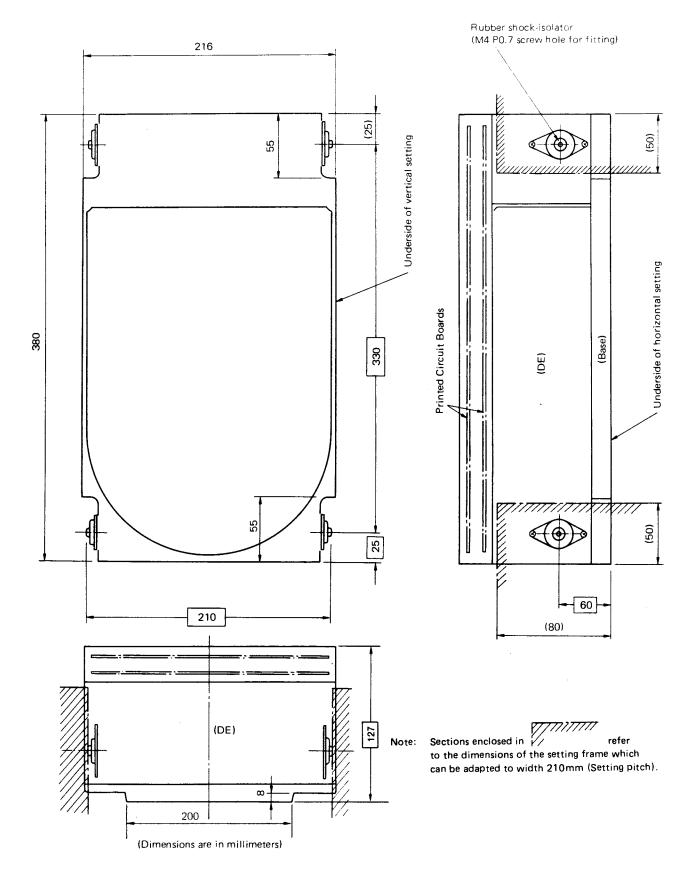
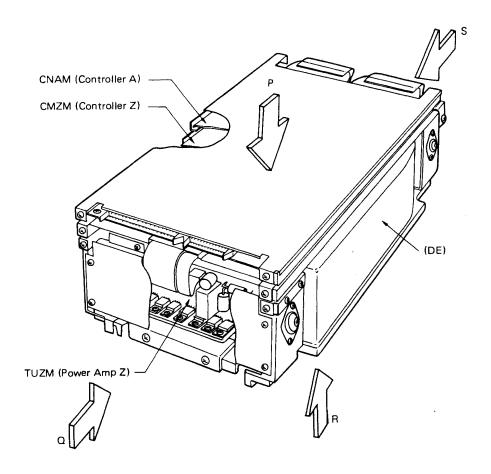


Figure 3-4-1 Mounting Dimensions of the Unit

3.4.2 Service Area

Maintenance, securing for transportation, cable connection, are accessed as shown below.

When determining the service area and where to install the locker, make sure that there is enough room for maintenance work.



P side: Maintenance operation on PCB (CNAM, CMZM)

Q side: Maintenance operation on PCB (TUZM)

Cable connections

R side: Securing the unit. (Refer to 4-3)

Accessing the VCM lock knob to secure the VCM.

S side: Securing the unit. (Refer to 4-3)
Operating the panel unit (Optional)

Figure 3-4-2 Maintenance Access on the Unit

3.4.3 Unlocking the Actuator

The actuator is locked during shipment: if rotates when the disks are stopped, the heads and disks may be damaged.

After installing the unit, the actuator must be unlocked by turning the knob on the bottom rear of the disk enclosure (DE). When the convex portion of the latch meshes with the concavo portion at the OFF position by turning the knob, the VCM (actuator) is unlocked. Refer to Figure 3-4-3.

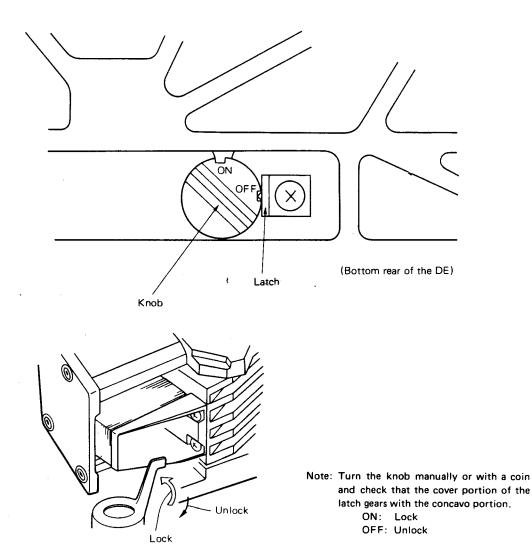


Figure 3-4-3 Locking/Unlocking the Actuator

3.4.4 Securing the Unit

In installing the unit, it is important that an unit does not touch any other hard parts such as mounting plate operating as well as non-operating (both storage and shipping).

To use this purpose, the unit is provided screw holes on Q side and S side (refer to Figure 3-4-2).

The holes are used to secure the unit to the mounting frame during shipment. Examples of securing the unit are shown in Figure 3-4-4 and Figure 3-4-5.

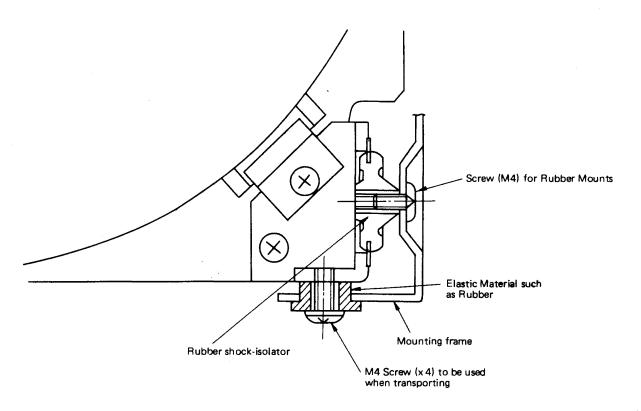
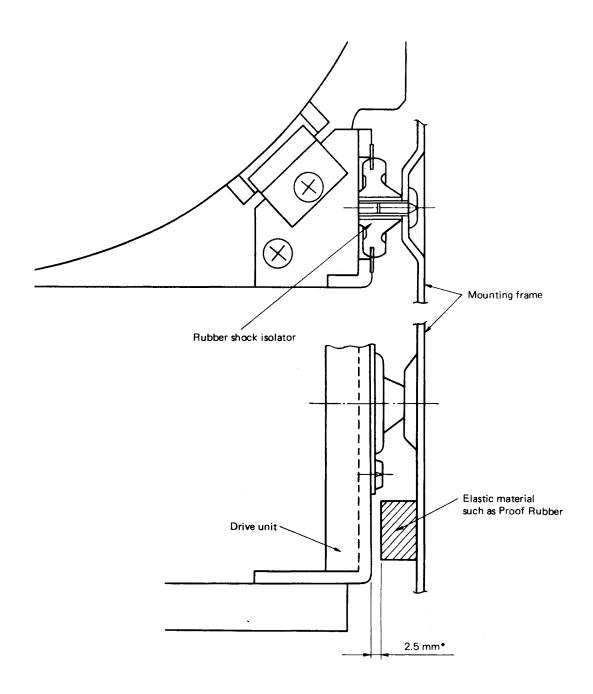


Figure 3-4-4 Securing the Unit (Example 1)

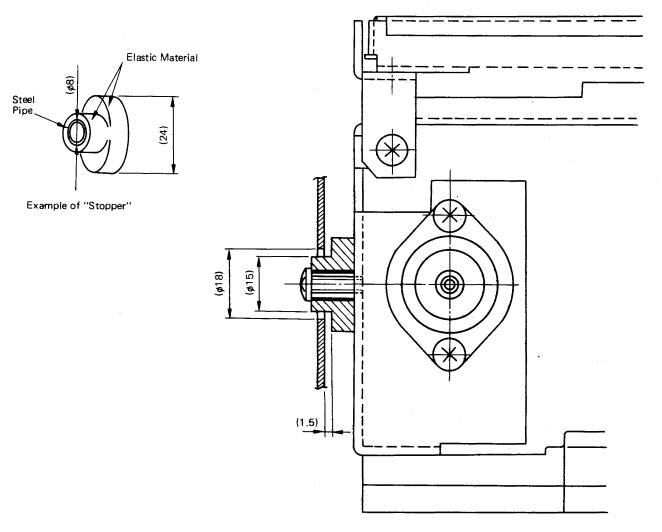


^{*} Maintain this gap so as while not to contact the drive unit if it vibrates at operating.

Figure 3-4-5 Securing the Unit (Example 2)

Moreover, in a effective way, the holes are used to attach some elastic materials for the stopper. The stopper plays a part as a shock absorber. And keeping a suitable clearance, the stopper protects not only a device but also rubber shock-isolators from damage. Figure 3-4-6 shows recommended form of the stopper. This stopper is effective when operating as well as non-operating, and needless to remove after shipping.

The screw hole dimensions on the unit are shown in Figure 3-4-7.



Note: That kind of stopper also can be attached on the optional fan unit. (Refer to Figure 3-4-7 (3))

Figure 3-4-6 Form of the Stopper

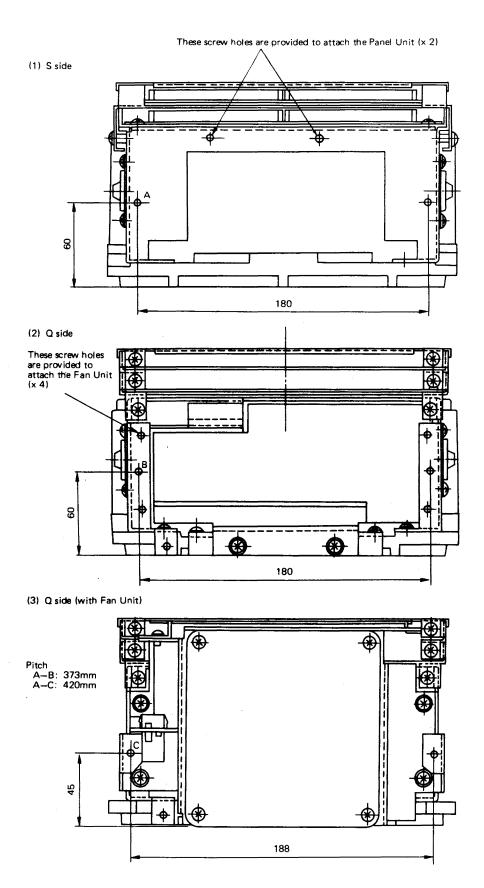


Figure 3-4-7 Dimensions of the Screw Holes

3.4.5 Cooling

This unit requires some means of cooling, since there is no internal blower motor. Figure 3-4-8 shows the recommended air flow posture.

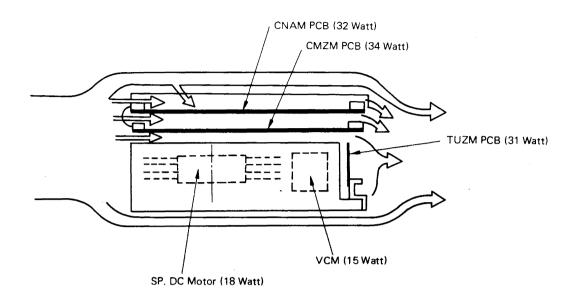


Figure 3-4-8 Recommended Air Flow Posture

* For this purpose, an optional fan unit is available. This fan unit will removes the generated heat most effectively. (Refer to 1.3.2.1)

The cooling condition can be confirmed by taking the surface temperature of some ICs and heat sinks.

The following IC's surface temperature must be kept under the temperature listed on the Table 3-4-1.

Table 3-4-1 Thermal Check Point

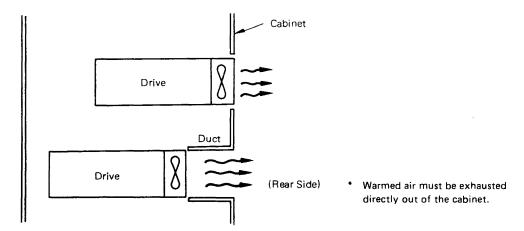
Part No.	On board	Maximum surface temperature (Tc)	
M165 (Linear IC)	CNAM PCB	85°C	
Q28 (-5.2V Tr)	CNZM PCB	85°C	
Q9 (Power Tr)	TUZM PCB	80°C	
Aluminum base (Bottom surface)	DE	55°C	

^{*} At random seeking

* Even on max. environment temperature (40°C).

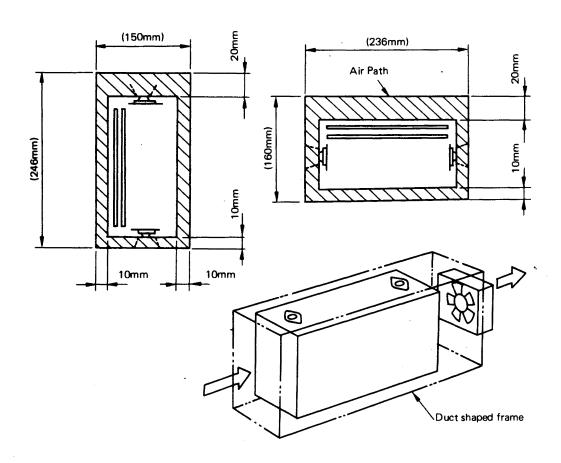
Figure 3-4-9 shows some examples of cooling installation.

(a) Using optional fan unit



(b) Without optional fan unit

We recommend that the installation frame is shaped like a duct and the cooling air flow path is illustrated as follows:



* Air flow rate of more than 1m³/min through the duct must be maintained.

Figure 3-4-9 Examples of Installation Cooling

3.5 MOUNTING OF OPTIONS

3.5.1 Mounting the fan unit

The optional fan unit can be mounted or replaced in the field. See Subsection 1.3.2.1 for the specifications, shape, and connector pin assignments of the fan unit. The mounting procedures of an optional fan are as follows:

- (1) Remove the protection cover from the power amplifier PC board (TUZM) at the rear of the equipment. (As the screws and washers are used to attach the fan, save the screws and washers after removing them from the order. The cover is not used when the fan unit is used.)
- (2) Mount the fan unit and attach it with the screws and washers from the protection cover. (Check that isolator bushes are in the four screw holes.)
- (3) Place the interface cables at the top of the fan unit. (The chloroethylene-coated hold cover can be removed by loosening the screws.)
- (4) Connect the power supply cable to the fan unit. Refer to Figure 3-5-1.

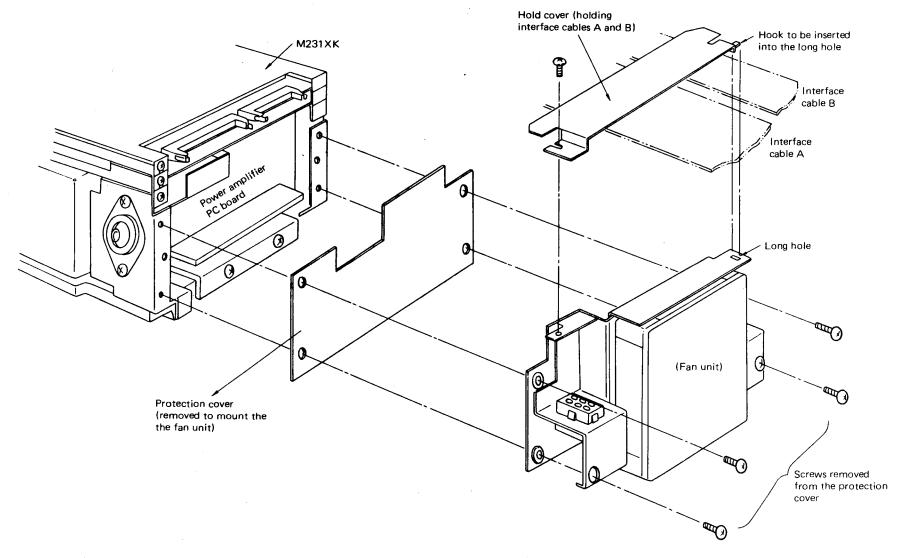
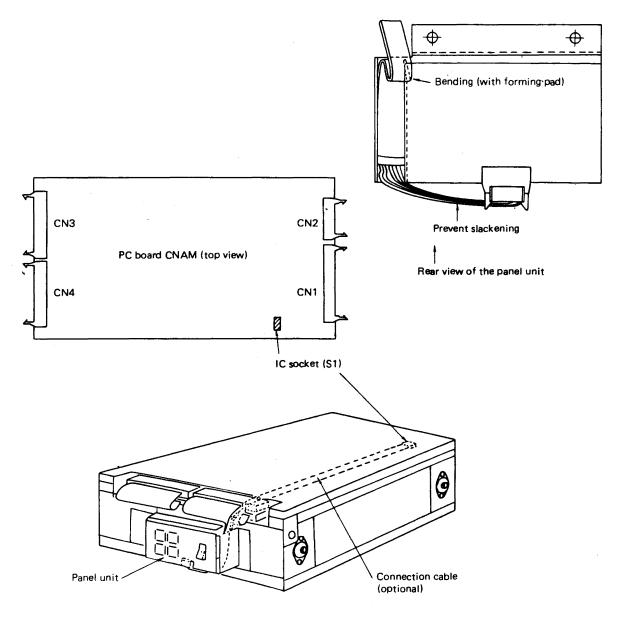


Figure 3-5-1 Mounting the Fan Unit

3.5.2 Mounting the Panel Unit

Figure 3-5-2 shows panel unit mounting diagrams.

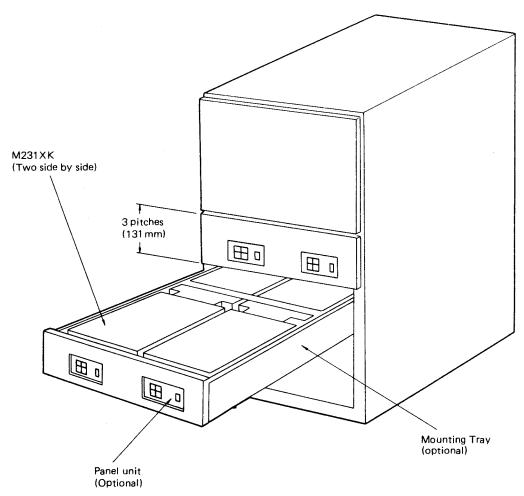


Note: To prevent the connection cable from slackening under the panel unit or on the equipment to p(PC board), bend the cable at the rear of the panel unit as in the figure at the right.

Figure 3-5-2 Mounting the Panel Unit

3.5.3 Installation Mounting Tray

Two disk drive units can be installed side by side, by 3 pitches (131mm) in height, on the 19-inch rack using the optional mounting tray as shown in Figure 3-5-3.



Note: Refer to Section 1-3-2-4.

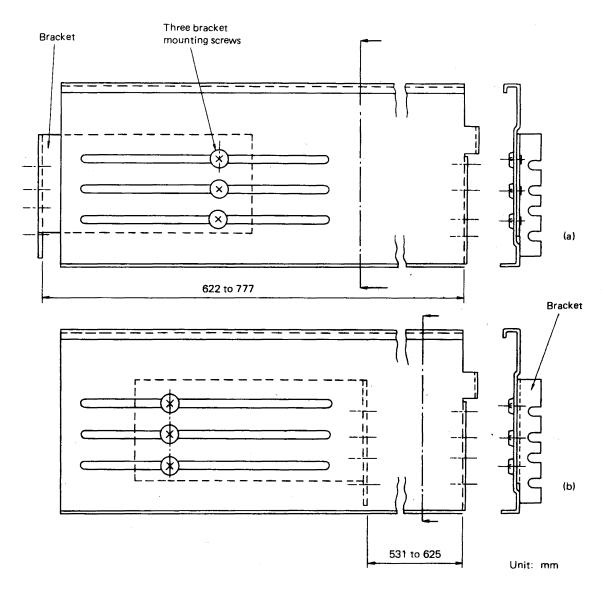
Figure 3-5-3 Installation in the 19-inch Rack

3.5.3.1 Installation Mounting Tray in the 19-inch Rack

First, mount the bracket assembly (B030-4590-T550) on the 19 inch rack as follows. The bracket assembly consists of a pair of right and left slide guides (outer rails).

- (1) Loosen 3 screws which hold the bracket in the back, so that it moves back and forth. (See Figure 3-5-4.)
 - The installation frame can be mounted in the 19 inch rack with a dpeth of mounting pitch ranging from 531 mm to 777 mm by adjusting the brackets. When mounting the installation frame in the rack with a depth of 622 mm to 777 mm, secure the brackets as shown in Figure 3-5-4 (a).
 - For racks other than the above, secure the brakets as shown in Figure 3-5-4, (b). The brackets are symmetrical, so a pair can be used for either (a) or (b).
- (2) Remove tapped plates and hold them on the 19-inch rack post as shown in Figure 3-5-5, (a).
- (3) Install left and right outer rails (bracket assembly) in the 19-inch rack. Tighten the bracket mounting screws after adjusting bracket location to fit it to the depth of the mounting pitch. (See Figure 3-5-5, (b).)

(4) Mount the outer rails using tapped plates with the bracket U-slots (in the back and front) pressed against the tapped plate fixing screws. (See Figure 3-5-5, (c).)



Note: The above figure ((a) and (b)) shows only the right slide guide (see from the front). The brackets in (a) and (b) are symmetrical to each other.

Figure 3-5-4 Bracket Assembly

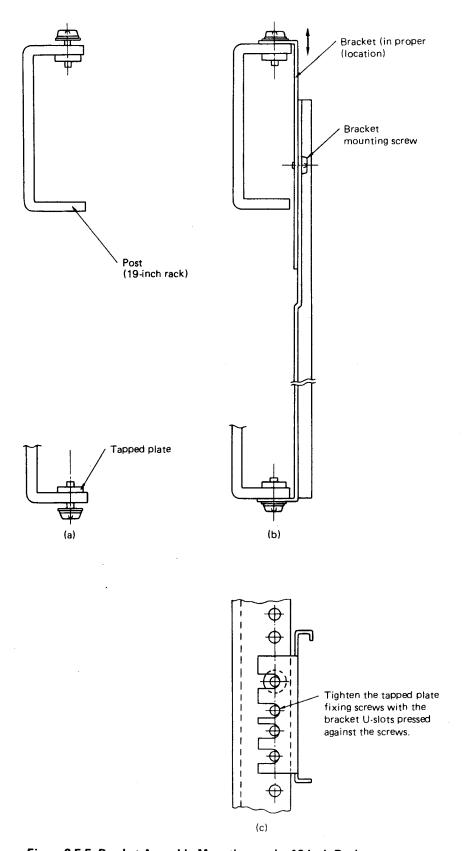


Figure 3-5-5 Bracket Assembly Mounting on the 19-inch Rack

- (5) Insert the mounting tray (inner rail) and check its movement. If it does not slide freely, loosen the tapped plate holding screws and adjust outer rail locations for their relative width.
 - Confirm that the inner rail stops against the stopper when it is pulled out. (The installation frame can be pulled out approximately 595 mm.)
- (6) Insert the mounting tray and fix it to the outer rails at the front left and right. (See Figure 3-5-6).
- (7) Mount the front panel.

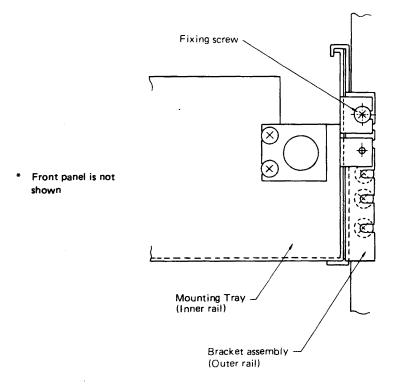


Figure 3-5-6 Mounting Tray to the Outer Rails

3.5.3.2 Each Unit Installation on the Mounting Tray

- (1) Fan unit installation
 - Disk drive units installed on the Mounting Tray must have a fan unit. Refer to Section 3.5.1.
- (2) Disk drive unit (with fan) installation
 - (A) Mount the rubber cushions, attached to the Mounting Tray, using taps in the front and back of the drive unit as shown in Figure 3-5-7.

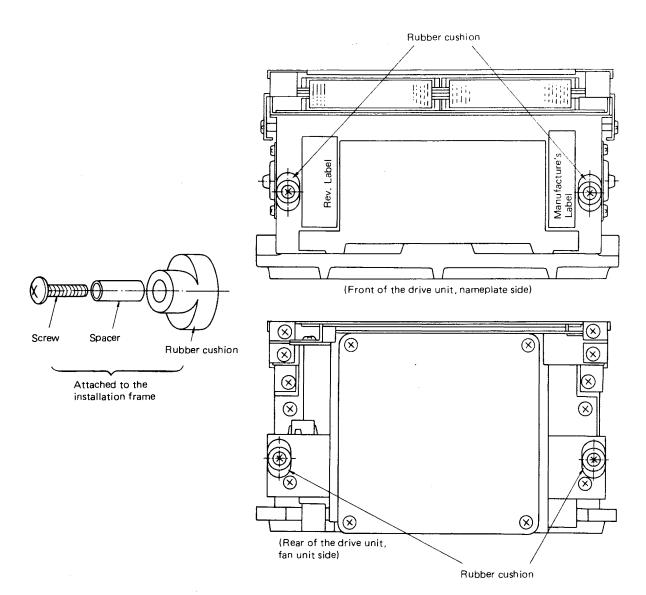
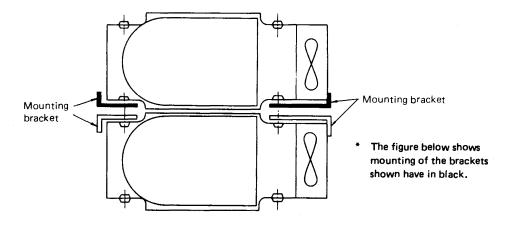
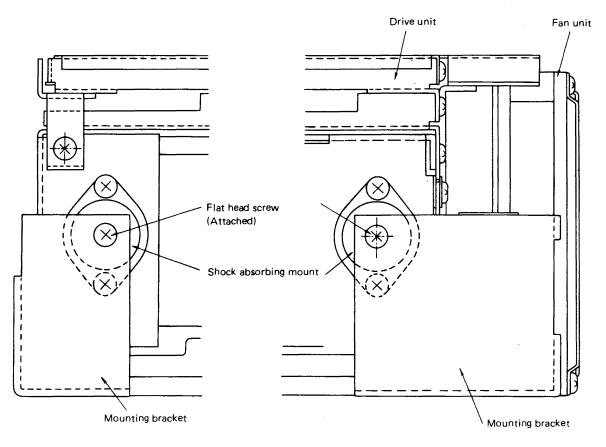


Figure 3-5-7 Rubber Cushion Mounting

- (B) Attach the mounting brackets using taps (M4) for shock absorbing mounts after setting the mounting brackets to disk drive unit location. Note that the front and back brackets are different. Refer to Figure 3-5-8.
- (C) Remove the cushion supports from the Mounting Tray. (4 per installation frame (See Figure 3-5-9.)
- (D) Set the disk drive on the Mounting Tray. The disk drive unit can temporarily ride on the front and back beams of the installation frame (inner rail) without manual support using the mounting brackets and 4 cushion supports in the front and back. (See Figure 3-5-10.) Therefore, even one person can install the drive unit on the Mounting Tray either removed or on the rack (pulled-out).

In this state, attach each shock absorbing mount (For the inside shock absorbing mount section, attach the mounting brackets already attached on the shock absorbing (mounts.) See Figure 3-5-10.

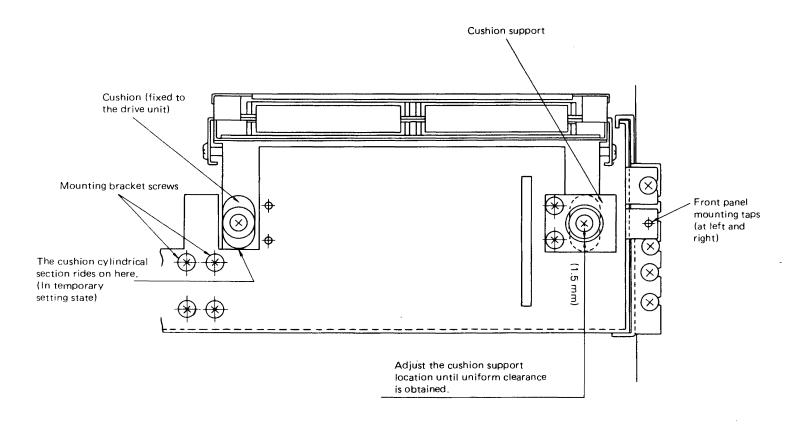




(a) Mounting in the front of the drive unit

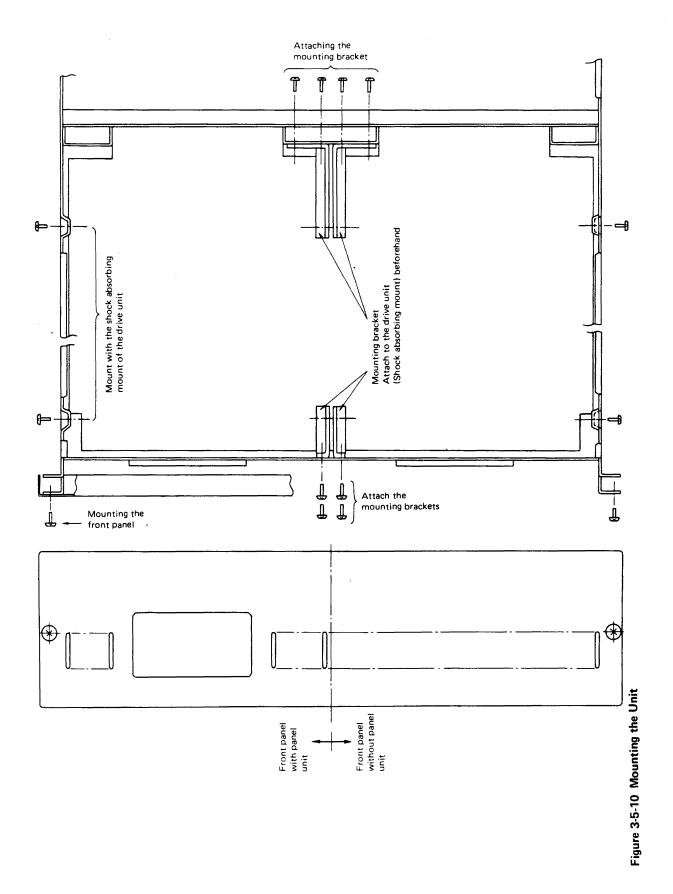
(b) Mounting in the back of the drive unit

Figure 3-5-8 Bracket Mounting



* The figure shows the right drive unit (seen from the front). The cusion supports of the left drive unit and the back (fan side) are the same.

Figure 3-5-9 Cushion Support



- (E) Mount the cushion supports that were removed in procedure (C), so that clearances around the stopper including those in its front and back are 1.5 mm. See Figure 3-5-9.
- (F) If the panel unit is required, mount it. See Item (3).
- (G) Mount the front panel.
- (3) Mounting the panel unit

The panel unit (optional) is mounted as shown in Section 3.5.2. When the panel unit is used in the Mounting Tray, mount it as shown in the following figure.

When the panel unit is mounted, use the Mounting Tray (B030-4590-T501) as the inner rail. (Refer to Section 1.3.2.4.) This type of Mounting Tray has a blank panel on one side. When installing 2 drive units, this blank panel is not used. When installing 1 drive unit, mount this blank panel in the unused window.

- Notes: 1. The protection cover on the installation frame edge protects cables from damage. Mount is together with the panel unit as shown in the following figure.
 - 2. For cable forming, see Figure 3-5-2.

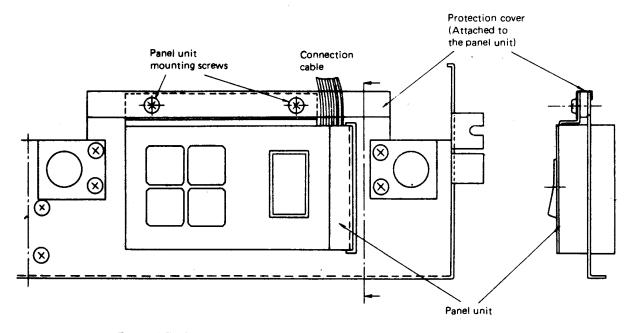
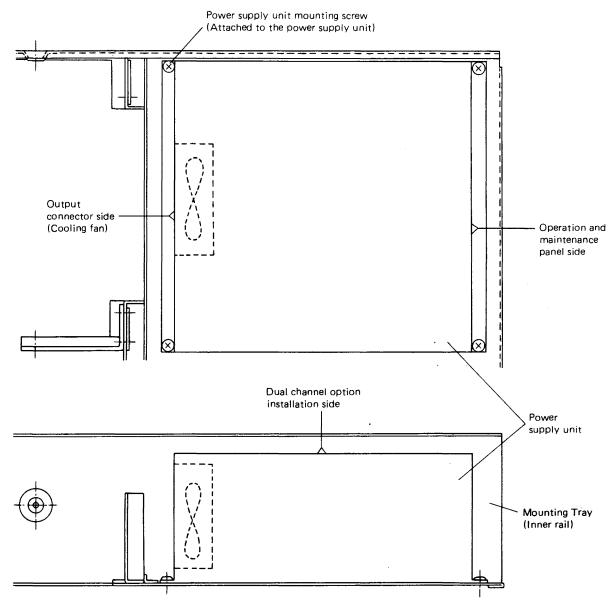


Figure 3-5-11 Mounting the Panel Unit

(4) Power supply unit installation

The power supply unit is mounted at the back of the Mounting Tray (inner rail) using 4 screws. Even after the inner rail is mounted on the 19-inch rack, the power supply unit can be installed if sufficient space is left.



Note: Refer to Section 1.3.2.5 for optimum cable lengths when the optional power supply unit is installed.

Figure 3-5-12 Power Supply Unit Installation

- (5) Dual channel option installation
 - The dual channel option can be mounted on the power supply unit. (Tap locations for mounting are shown in Figure 1-3-5.)
 - (A) Mount the bracket (2a) on the rail (1a) using screws SBD M3x5. The left and right brackets and rails are symmetrically mounted.
 - (B) Mount the spring (3a) on the rail (1a) using screws SBD M2x5. The left and right brackets and rails are symmetrically mounted.
 - (C) Mount the rails (1a) on the power supply unit using screws SSA M4x8.
 - (D) Mount the guide (4a) at the back (operating section) of the power supply unit using screws SBD M4x8.

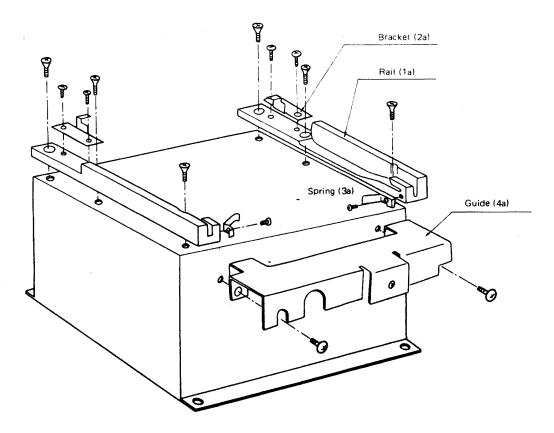


Figure 3-5-13 Dual Channel Option Installation 1

(E) Mount the dual channel PC board on the frame (6a) using screws SBD M3x5. (See Figure 3-5-14.)

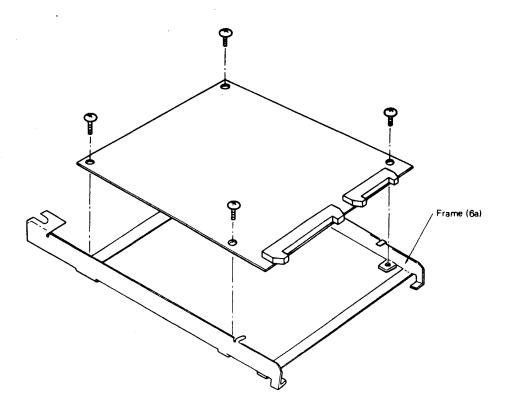


Figure 3-5-14 Dual Channel Option Installation 2

(F) Pressing PC board unit (PC board and frame assembly) (12a) downward, insert it until the springs deflect slightly. The PC board unit frame is automatically latched at lugs of the brackets (2a) and locked. (See Figure 3-5-15.)

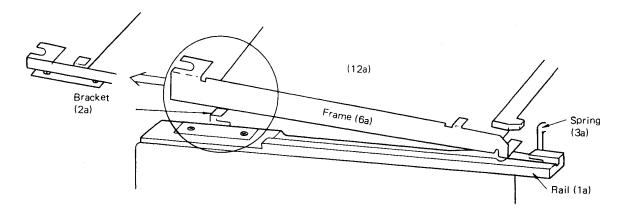


Figure 3-5-15 Dual Channel Frame Mount

- (G) Connect CN25 on the PC board and CN33 on the power supply unit with the connection cable (B660-0625-T329A). (See Figure 3-5-16.)
- (H) Connect interface cables (8a and 9a) between the drive unit (CNAM) and the dual channel PC board.
- (I) Connect the A-channel cable B to the PC board, and pull the cable out behind the power supply unit.
- (J) Remove the dual channel PC board from the rails and connect the A-channel cable A to the drive unit (CNAM), and pull the cable out under the dual channel PC board and behind the power supply unit.
- (K) Connect B-channel cables A and B to the back of the PC board (CN21 and CN22) and pull them out behind the power supply unit.

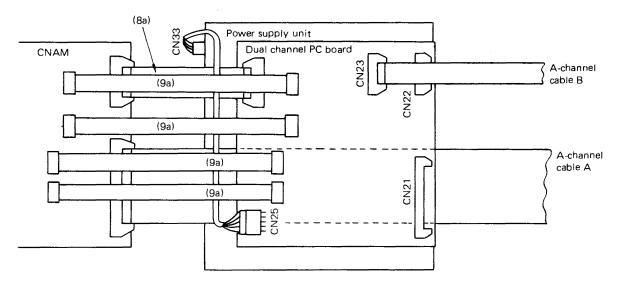


Figure 3-5-16 Dual Channel Cabling

(L) Attach the cover (11a) on the frame (6a) using screws SBD M3x5.

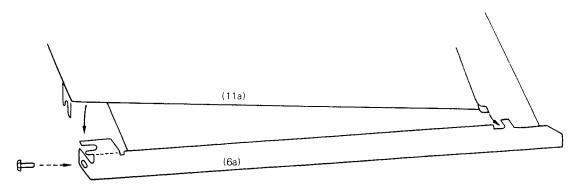


Figure 3-5-17 Dual Channel Top Cover Fixing

(M) Form the A- and B-channel interface cables along the guide (4a) and hold them with the cable retainer (13a).

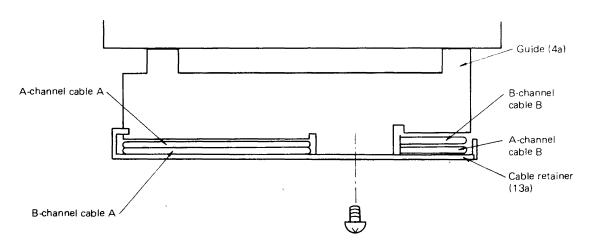


Figure 3-5-18 Dual Channel Interface Cables Holding

* Part number of the dual channel option is B03B-4590-E401A.

3.5.4 Mounting the Dual Channel Option

The procedure for mounting the dual channel option on the power supply (procedure B03B-4590-E401A) was previously described in Subsection 3.5.3.2. This subscription describes the procedure for mounting the option on the drive unit (procedure B03B-4590-E402A).

- (1) Remove the cover (PC board protection cover) from the drive unit. (See Figure 6-5-2.)
- (2) Mount the dual channel BCB on frame 6a as shown in Figure 3-5-14.
- (3) Connect the drive unit (CNAM) to the PC board via the cable as shown in Figure 3-5-16.
- (4) Insert cover 1b between frame 6a and the equipment from the front of the equipment. Replace the cover on the drive unit as for the protection cover.
- (5) Insert frame 6a with the PC board into the four supporting arms on cover 1b. Fix the frame with two screws (M3x5). Place frame tangs 2b under the supporting arms. (See Figure 3-5-17).
- (6) Connect cable B to channel A (CN23).
- (7) Attach cover 3b in the frame of cover 1b with screws.

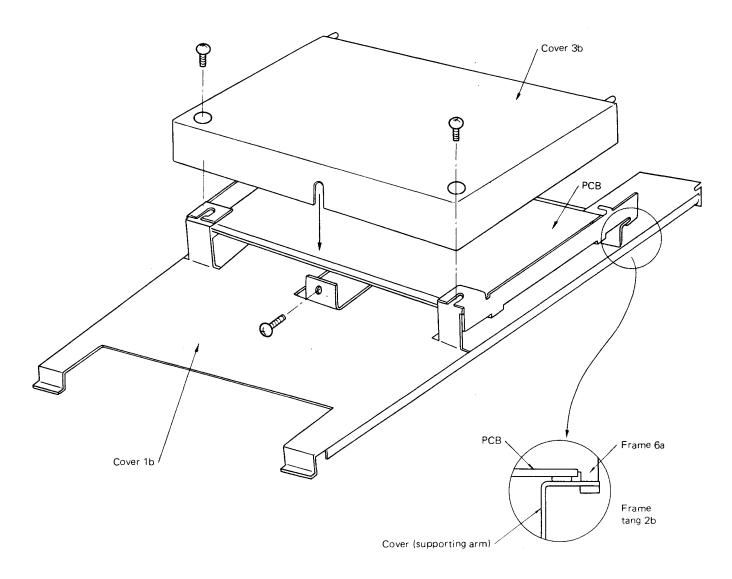


Figure 3-5-19 Mounting the Dual Channel Option

- (8) Connect all other interface cables to channels A and B.
- (9) Remove the cable holder from the optional fan unit and attach cable duct 4b, which is an accessory of the dual channel option, to the unit. The duct is attached in the same way as for the cover to the fan unit.
- (10) Extend the interface cables and power cable from the rear of the equipment to holder 3b. (See Figure 3-5-18.)

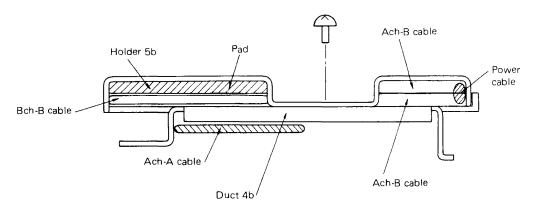


Figure 3-5-20 Dual Channel Cables Holding

3.5.5 Dual Channel Option Configuration

There are two kinds of dual channel options. One is installed on the power supply and the other is installed on the drive. The parts configuration of each option is as follows:

Table 3-5-1 Dual Channel Option

	Option P/N Description		Configuration on PSU B030B-4590-E401A	Configuration on Drive B030B-4590-E402A
1	Frame Assembly	1	B030-4590-V401A	B030-4590-V402A
2	PCA (XCDM) (SMD)	1	B16B-7990-0060A	B16B-7990-0060A
3	Small Screw	4	F6-SBD-3X5S-M-Ni1A	F6-SBD-3X5S-M-Ni1A
4	Cable 1	4	B660-1060-T096#L2R602	B660-1060-T096#L2R802
5	Cable 2	1	B660-1060-T097#L1R602	B660-1060-T097#L3R002
6	Label	1	B370-1360-0094A	B370-1360-0095A B370-0950-0340A B370-0950-0341A B370-0950-0342A B370-0950-0343A
7	Power Supply Cable	1	B660-0625-T329A#L3R002	B660-0625-T329A#L1R503
8	Strain Relief	1		

3.6 CABLING

3.6.1 Connectors On Unit Side

Figure 3-6-1 shows the mounting positions of the connectors on the M231XK.

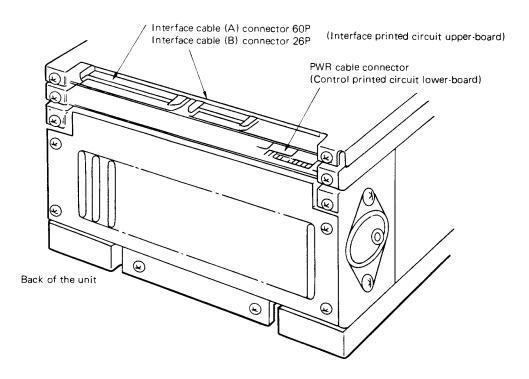


Figure 3-6-1 Mounting Positions of Connectors

Cables include an interface (A) cable 60P, an interface (B) cable 26P, and a power cable

Refer to Section 3.6.2 for additional information on the power cable.

3.6.2 Power Cable Connection

The M231XK uses only the DC power, Connector specification for the unit, recommended specifications for the cable, and pin assignment and voltages follows.

- (1) Specification on the unit side
 - Header C63L-0820-0008 (2420-07A-G manufactured by Molex Japan Co., Ltd.)

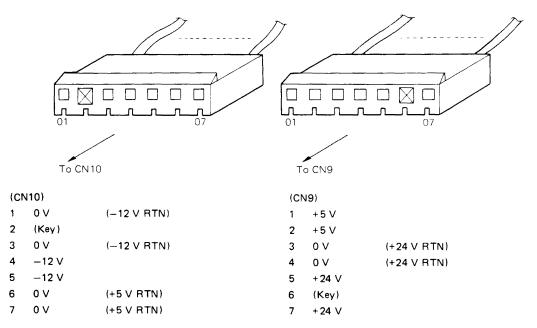
(7P) x 2 units

- (2) Recommended specifications on the cable side
 - Housing C63L-0820-0007 (2139-7 manufactured by Molex Japan Co., Ltd.)
 (7P) x 2 units
 - Contact C63L-0820-0002 (2478-GL manufactured by Molex Japan Co., Ltd.)

(12 units)

Key C63L-0820-0001 (2560-1 manufactured by Molex Japan Co., Ltd.)
 (2 units)

(3) Pin assignment and voltages Refer to Figure 3-6-2.



Note: 1 Use AWG18 as the cable material.

- 2 The cable length must be less than 1.5m.
- 3 All "OV" must be connected together at power supply outputs.

Figure 3-6-2 Pin Assignment and Voltages

If the power supply (option: B14L-5105-0100A) is used, a power cable is provided. (refer to Figure 3-6-3)

Specify the length of the power cable as follows [for 50 cm (example)]:

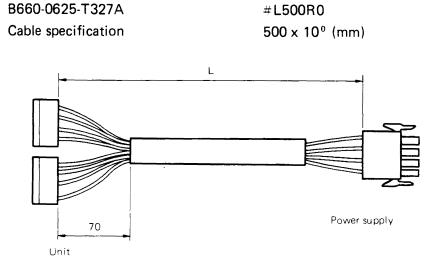


Figure 3-6-3 Power Cable (Specification: B660-0625-T327A)

3.6.3 Interface Cabling

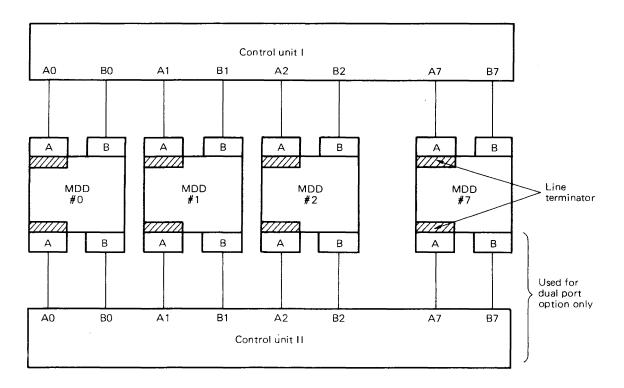
Interface cables include cable (A) (60P) for control signals and cable (B) (26P) for data signals.

(1) Cabling

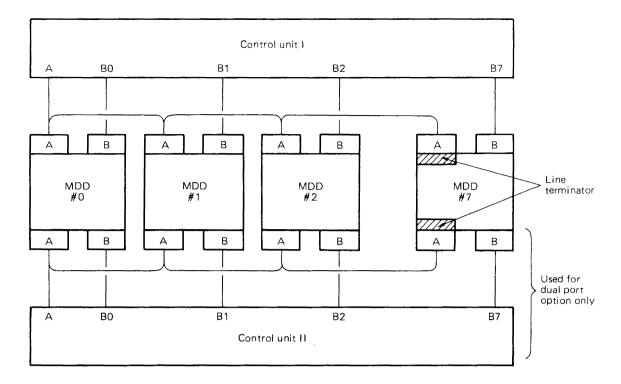
Cables are connected with the system in the star-chain mode or the daisy-chain mode, as shown in Figure 3-6-4. For the star-chain mode, the line terminator for cable (A) is necessary for every device. For the daisy chain mode only the last device requires a line terminator.

The unit side of cables (A) and (B) use lights angled connectors which have no malinsertion preventive keys. Insert the cable to match the triangular marks on the connectors, (at the number one) shown in Figure 3-6-5. Then lock them from both sides with the locking lever.

If an optional fan unit is used, fix cables (A) and (B) at the upper section of the fan unit, as shown in Figure 3-5-18.



a) Star-chain cabling



b) Daisy-chain cabling

Figure 3-6-4 System Interface Cabling

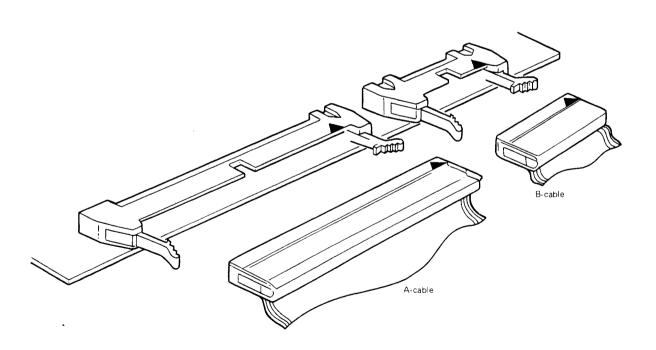


Figure 3-6-5 Interface Cabling

(2) Cable Termination

In the daisy-chain configuration, (A) cable signals must be terminated at the last disk drive with four IC module-resistors packs as shown in Figure 3-6-6. The four IC module resistors packs are installed in all disk drives; therefore they must be removed from the disk drives on which the line termination is unnecessary.

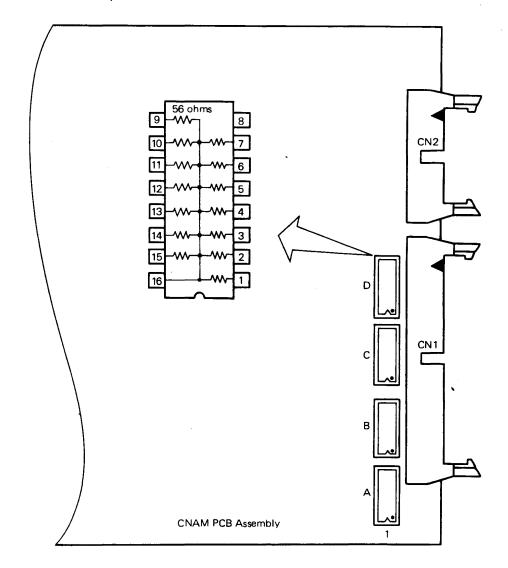


Figure 3-6-6 Cable Termination

3.6.4 System Grounding

(1) These M231XK is uniformly grounded at the signal ground (SG) connector. If SG connection is required on the system, use the SG tap at the back of the unit, shown in Figure 3-6-7.

The optional fan unit is grounded at the FG (Frame ground) connector, the SG (Signal ground) is separated from the FG (Frame ground) with insulating bushings.

A grounding cable may be connected as shown in Figure 3-6-8, if it is required.

(2) The FG and SG terminals are provided with the optional power supply unit. Connecting or disconnecting FG and SG on the power supply unit can be

performed according to system power distribution and system ground requirements.

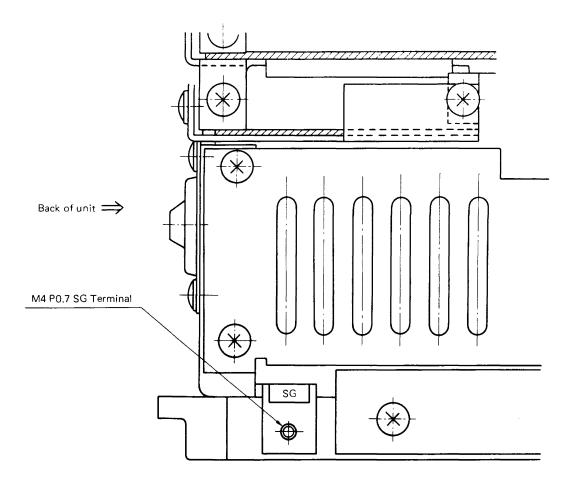


Figure 3-6-7 SG Terminal

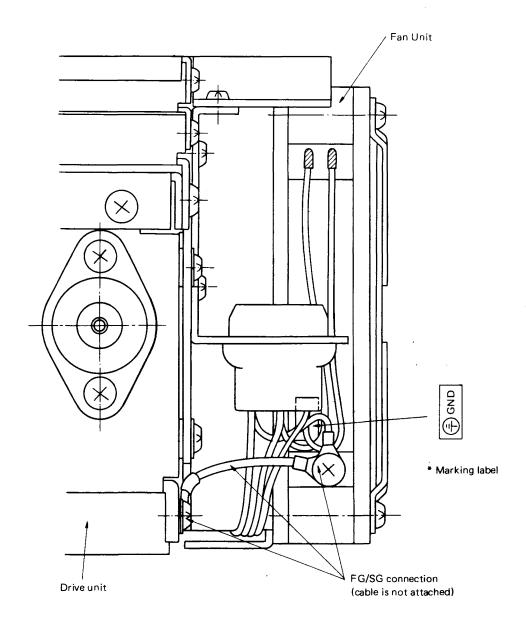


Figure 3-6-8 FG/SG Connection

3.7 MODE SELECT SETTING

When the M231X Micro Disk Drive is installed in the system, the customer must set switch 1 through 3 according to system requirements; these switches determine, Disk Logical Unit Number, Sector Mode, Tag 4/5 Enable, File Protect and Sector Counting, Switch 1 through Switch 3 is located on the CNAM PCB Assembly, as shown in Figure 3-7-1.

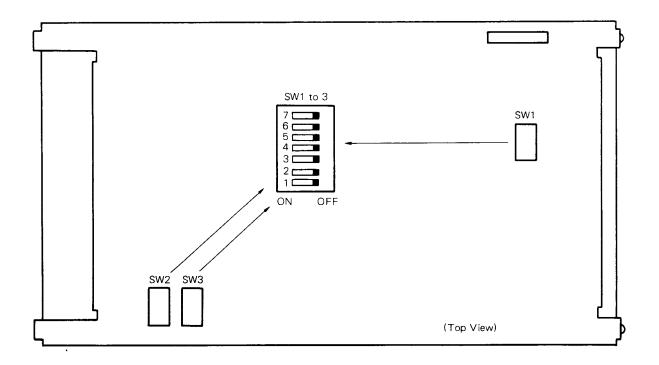


Figure 3-7-1 Mode Select Switch Location

3.7.1 Disk Addressing

Disk Logical Unit Number 0 to 7 is selected by SW1 at location E3 on the CNAM PCB assembly. Set the desired disk address with the three keys on SW1 using the binary code as shown in Table 3-7-1.

Table 3-7-1 Disk Addressing

Disk Address	Key 1	Key 2	Key 3
DISK Address	2 ¹	2 ²	2 ³
0	OFF	OFF	OFF
1	ON	OFF	OFF
2	OFF	ON	OFF
3	ON	ON	OFF
4	OFF	OFF	ON
5	ON	OFF	ON
6	OFF	ON	ON
7	ON	ON	ON

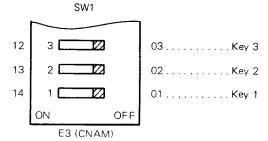


Figure 3-7-2 Disk Addressing

3.7.2 Sector Mode

The customer can select Hard Sector mode (1 to 128 sectors) or Variable Soft Sector mode, using Key 6 on SW1 at location E3 on the CNAM PCB assembly according to Table 3-7-2 as shown in Figure 3-7-3.

In the case of Hard Sector, the customer must set the number of sectors per disk revolution as described in Section 3.7.5. Setting the number of sectors per revolution is also available in the Variable Soft Sector mode.

Table 3-7-2 Sector Mode

Sector Mode	Key 6
Hard Sector	OFF
Variable Soft Sector	ON

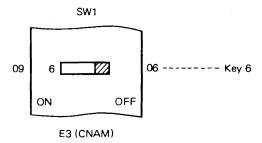


Figure 3-7-3 Sector Mode

3.7.3 Tag 4/5 Enable

The M231XK provides optional Tag 4 and Tag 5 functions. The customer may disable or enable these optional functions using Key 5 on SW1 at location E3 on the CNAM PCB assembly. Refer to Figure 3-7-4. Disabling the Tag 4 and Tag 5 functions inhibits the receivers of Tag 4 and Tag 5 receivers on the interface.

Table 3-7-3 Tag 4/5 Enable

Tag 4/5	Key 5
Disable	OFF
Enable	ON

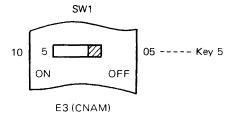


Figure 3-7-4 Tag 4/5 Enable

3.7.4 File Protect

When the customer desires to inhibit the write operation, the File Protect key may be set to the On position, using Key 7 on SW1 at location E3 on CNAM PCB assembly. Refer to Figure 3-7-5.

Table 3-7-4 File Protect

File Protect	Key 7
Enable writing	OFF
Disable writing	ON

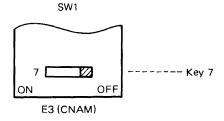


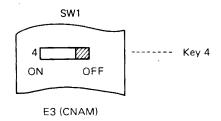
Figure 3-7-5 File Protect

3.7.5 Device Type (optional)

The device type, M2311K or M2312K, can be selected by setting key 4 on SW1.

Table 3-7-5 Device Type

Device Type	Key 4
M2311	OFF
M2312	ON



Note) Tag 4/5 feature must be enabled to obtain device type code.

Figure 3-7-6 Device Type

3.7.6 Sector Counting

Sector count configuration switches SW2 and SW3 are located at A26 and A24 respectively on the CNAM PCB assembly. Each key of SW2 and SW3 represents the binary powers of the Byte Clock as shown in Table 3-7-6.

Table 3-7-6 Sector Counting Keys

SW2 Key No.	Value	SW3 Key No.	Value
1	1	1	128
2	2	2	256
3	4	3	512
4	8	4	1024
, 5	16	5	2048
6	32	6	4096
7	64	7	8192

(1) Calculation based on Sectors/Track

$$\frac{20,480}{\text{Number of sectors}} = \frac{\text{EXAMPLE}}{\text{(Calculations for 9 Sectors)}}$$

$$\frac{20,480}{\text{per sector}} = \frac{20,480}{9} = 2,275.555$$

 If the above calculation results in a remainder, truncate the remainder and add one to the integer portion of "number of bytes per sector".

EXAMPLE (Calculations for 9 Sectors)

3) Configure SW2 and SW3 to "number of bytes per sector" minus one to allow for sector counter reset clock.

$$2,276 - 1 = 2,275$$

4) To determine how many by bytes (if any) the last sector of each track will be short, multiply "number of bytes per sector" by "number of sectors" and subtract 20,480.

Last sector short 4 bytes

(2) Calculation based on Bytes/Sector

Example: 583 Bytes/Sector

2) Select the keys must be OFF position referring to Table 3-7-6 after the following calculation.

3) Calculate the Sectors/Track

Sectors/Track =
$$\frac{\text{Bytes/Track}}{\text{Bytes/Sector}}$$
$$= \frac{20,480}{583}$$
$$= 35,129$$

4) If the above calculation results in a remainder, truncate the remainder. The integer portion means actual sectors per track.

Actual Sectors/Track = 35

5) Calculate the number of the last sector (remainder).

Last Sector Length =
$$20,480 - (Bytes/Sector) \times (Sectors/Track)$$

= $20,480 - 583 \times 35$
= 75

Table 3.7.7 Sector Selection

0	SW2	SW3	D.4s/Conto	Last Sector
Sector	1 2 3 4 5 6 7	1234567	Byte/Sector	Shorter
1			20,480	0
2	111111	1111001	10,240	0
3	0101010	1010110	6,827	-1
4	111111	1110010	5,120	0
5	111111	1111100	4,096	0
6	1010101	0101100	3,414	-4
7	1011011	0110100	2,926	-2
8	111111	1100100	2,560	0
9	1100011	1000100	2,276	-4
· 10	1111111	1111000	2,048	0
11	1010001	0111000	1,862	-2
12	0101010	1011000	1,707	-4
13	1110010	0011000	1,576	-8
14	0110110	1101000	1,463	-2
15	1010101	0101000	1,366	-10
16	111111	1001000	1,280	0
17	0010110	1001000	1,205	-5
18	1000111	0001000	1,138	-4
19	1010110	0001000	1,078	-2
20	1111111	1110000	1,024	0
21	1111001	1110000	976	-16
22	0100010	1110000	931	-2
23	0101111	0110000	891	-13
24	1010101	0110000	854	-16
25	1100110	0110000	820	-20
26	1100100	0110000	788	-8
27	0110111	1010000	759	-13
28	1101101	1010000	732	-16
29	0100001	1010000	707	-23
30	0101010	1010000	683	-10
31	0010100	1010000	661	-11
32	111111	0010000	640	0
33	0011011	0010000	621	-13
34	0101101	0010000	603	-22
35	1001001	0010000	586	-30
36	0001110	0010000	569	-4
37	1001010	0010000	554	-18
38	0101100	0010000	539	-2
39	1011000	0010000	526	-34

Table 3.7.7 Sector Selection (Continued)

	SW2 2	SW2 3		
Sector	1234567	1234567	Byte/Sector	Last Sector Shorter
40	111111	1100000	512	0
41	1100111	1100000	500	-20
42	1110011	1 1 0 0 0 0 0	488	-16
43	0011101	1100000	477	-31
44	1000101	1100000	466	-24
45	1 1 1 0 0 0 1	1100000	456	40
46	1011110	1100000	446	-36
47	1100110	1100000	436	-12
48	0101010	1100000	427	-16
49	1000010	1100000	418	-2
50	1001100	1100000	410	-20
51	1000100	1100000	402	-16
52	1001000	1100000	394	8
53	0100000	1100000	387	-31
54	1101111	0100000	380	-40
55	0010111	0100000	373	-35
56	1011011	0100000	366	-16
57	1110011	0100000	360	-40
58	1000011	0100000	354	-52
59	1101101	0100000	348	-52
60	1010101	0100000	342	-40
61	1 1 1 1 0 0 1	0100000	336	-16
62	0101001	0100000	331	-42
63	1010001	0100000	326	58
64	1111110	0100000	320	0
65	1101110	0100000	316	60
66	0110110	0100000	311	-46
67	1000110	0100000	306	-22
68	1011010	0100000	302	56
69	0001010	0100000	297	-13
70	0010010	0100000	293	-30
71	0000010	0100000	289	-39
72	0011100	0100000	285	-40
80	111111	1000000	258	0
128	1111100	1000000	160	0

- Notes: (1) "1" indicates that the key is set to ON side.
 - (2) "0" indicates that the key is set to OFF side.
 - (3) The last sector is equal or shorter than nominal sector.

3.8 SHIPPING

Perform the following operations when the M231XK is to be shipped mounted in a 19-inch rack.

- (1) Lock the actuator (refer to Section 3.5).
- (2) Secure the unit:

We recommend to attach a elastic material to the mounting-frame side near the rubber shock-isolator, so that excessive force is not applied to the isolators.

- Refer to 3.4.4 for securing the unit. When the unit is shipped by itself, the same operation (1) is required before packing into the proper carton.
- (3) This process is required so that the shock applied to the unit during shipment exceed 5G.

3.9 STORAGE AND REPACKING

When reshipping the unit, lock the actuator and repack it in the original carton or a carton having equivalent functions.

When the environmental is conditions are severe and the unit is to be stored for an extended period of time, it should be packed in its box.

Units can be stacked three cartons high.

When storing unpacked units, avoid locations that are dusty or subject to extreme environmental changes are extreme.

Section 4 **Theory of Operation**

4. THEORY OF OPERATION

4.1 GENERAL DESCRIPTION

The operation of the M231XK is divided into three parts. The first part (Section 4.2) describes the mechanical assemblies of the unit. The second part (Section 4.3 and 4.4) describes the magnetic heads and magnetic disks. The third part (Section 4.5 and 4.6) describes the interface, servo circuit, R/W control, and other electronic controls.

4.2 MECHANICAL ASSEMBLIES

4.2.1 Disk Enclosure

The Disk Enclosure (DE) is a completely sealed unit containing the disks, spindle, actuator, and heads. Each of these are visible from the outside through a plastic cover. The DE is sealed at the factory and must not be opened in the field.

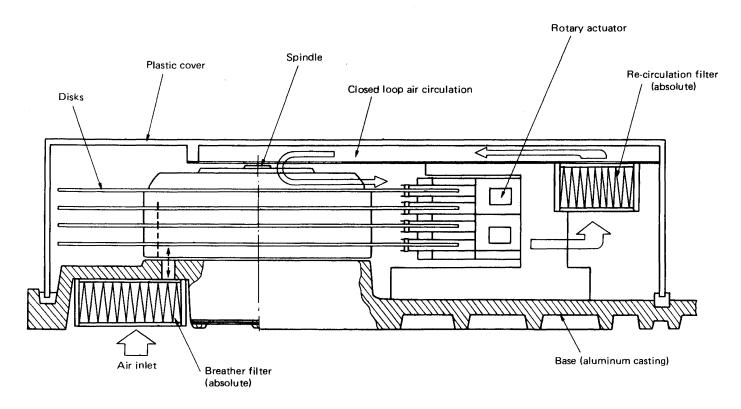
4.2.2 Air Circulation in DE

As the Contact stop/start (CSS) head used in this disk unit has a very low flying height (approximately $0.35\mu m$), head crashes can be caused by microscopic foreign particles. To keep the inside of the DE clean, the enclosure is completely sealed and clean air is supplied through two fileters. A breather is used for external air intake, while a re-circulation filter keeps the air inside the DE clean. Refer to Figure 4.2.1.

The breather filter is used for the following purposes:

- (a) Prevention of negative pressure in the vicinity of the spindle when the disk begins to rotate.
- (b) Prevention of dust intake when the air in the DE contracts due to a temperature difference between the DE and its environment.

The re-circulation filter, attached to the closed loop duct in the DE, is used to keep the air free of foreign particles. When a pressure difference is caused in the DE by the rotation of the spindle, the air in the DE circulates through the closed loop. Because it continually passes through this filter, the air is always kept clean. These two filters can remove 99.97% of the dust particles $(0.3\mu m \text{ min.})$.



Note: M3211 contains 3 disks in DE M3212 contains 4 disks in DE

Figure 4-2-1 Air Circulation Inside Disk Enclosure (DE)

4.2.3 Spindle/Drive Motor

The spindle/drive motor is an integral part of the chassis. It consists of seven major components: Shaft, Hub, Bearings, Stator, Rotor, Antistatic Brush, and Speed Sensor. Refer to Figure 4.2.2. The motor shaft is fixed within the motor housing by upper and lower bearings which are sealed to prevent contamination of the disk platter environment. The stator is fixed to the outer radius of the cast motor housing. The hub is fixed to the top of the motor shaft. The rotor and disk platters are fixed to the hub. The antistatic brush contacts the bottom of the motor shaft and dissipates any electrostatic noise to the chassis. A Hall-effect sensor detects the movement of the hub. The signal produced by this sensor is compared with an oscillator clock on the PCB in order to maintain the normal rotational speed of 3,600 RPM.

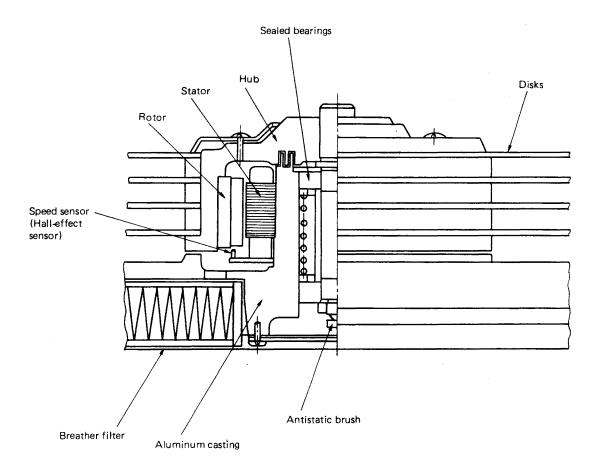


Figure 4-2-2 Spindle/Drive Motor

4.2.4 Actuator Arm Assembly

A low-power-consumption, rotary-type actuator is used to move the data heads and servo head along a circular arc to the specified cylinder. A moving coil is attached to the other end of the actuator arm and moves freely between fixed permanent magnets without contact. When current is applied to the coil, the coil and magnets interface and the actuator moves around the pivot. Refer to Figure 4.2.3.

The actuator performs the following types of motion, which are controlled by servo feed-back current from the servo head.

- (1) Seek
 - Heads are moved to the specified cylinder while counting track-crossing signals.
- (2) On Cylinder

Heads follow the specified tracks. The servo system prevents mispositioning due to disturbances such as shock, vibration, or temperature changes.

The servo head is located on the lower surface of the bottom disk, where servo information is pre-written at the factory.

This servo information is used as a control signal for the actuator; that is, it provides track-crossing signals during a seek operation, track-following signals during On Cylinder operation, and timing information such as index and servo clock.

The heads are incontact with the disk surfaces during start and stop (CSS heads) at a fixed position called the landing zone. This zone is on the innermost area of the disk, separate from the recording zone. A spring force holds or fixes the actuator at this position. If no current is applied to the moving coil, the heads are fixed at the landing zone to prevent head to disk without CSS in the recording zones.

Once the disks attain the required rotational speed, an initial seek frunction occurs. Current then flows in the coil and the heads are released from the landing zone and moved to Cylinder 0.

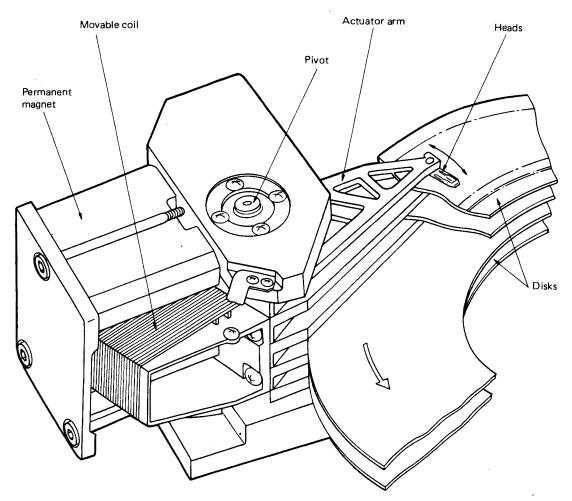


Figure 4-2-3 Actuator Arm Assembly

4.3 MAGNETIC HEADS AND RECORDING MEDIA

4.3.1 Magnetic Heads

To accomplish high density recording, Contact Start/Stop (CSS) flying heads are employed. The heads fly on the surface air flow generated by the rotating disk. The CSS system differs from the conventional ramp-load system in that the heads are always over the recording media and rest on the disk surface when the disk is not rotating.

Since, the head and disk make contact, the wear caused by this contact must be minimized. Therefore, the CSS heads are lightly loaded and surface pressure is reduced by using a tapered flat slider such as that shown in Figure 4-3-2. The slider has three rails. The air intake end of the slider is tapered to obtain from the air flowing over the disk surface. Read and write are performed by a ferrite core at the rear of the head, the minimum flying height position.

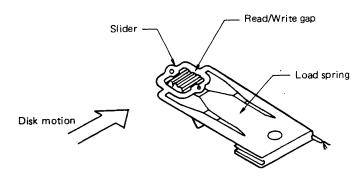


Figure 4-3-1 Read/Write Head

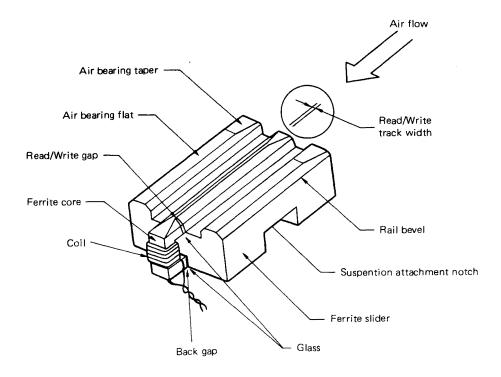


Figure 4-3-2 Tapered Flat Slider

4.3.2 Recording Media (Magnetic Disk)

The data recording media are aluminum disks approximately 200 mm (8 inches) in diameter and approximately 2 mm (75 mil) thick, and are coated with a magnetic material. Since the M231XK employs CSS heads, to prevent wear the surface is coated with a special material. Up to four disks can be installed for a maximum storage capacity of 84.4 MB. The bottom surface of the lowest disk is for the servo area, on which the positioning data and clock signals are recorded.

4.3.3 Servo Track Format

4.3.3.1 Servo track configuration

The servo area is used to store the unique data patterns which generate the Track Positioning, Index, Guard Band, and Clock signals. This data is pre-recorded on the disk before the unit is shipped from the factory.

The servo area consists of a combination of ODD1, ODD2, EVEN1 and EVEN2 tracks. The physical placement of servo tracks is shown in Figure 4-3-3. The servo tracks are divided into the following five parts:

- (1) Dead Space (DS or Landing Zone)
 - Dead Space is used for head contact during start and stop. DS consists of five DC-erased tracks and is recognized as Head Unloaded through the servo circuit.
- (2) Inner Guard Band 2 (IGB2)
 Inner Guard Band 2 is used for speed control during RTZ or Initial seek sequence. IGB2 consists of six EVEN1—EVEN2 tracks, six ODD1—EVEN2 tracks, six ODD1—ODD2 tracks and five EVEN1—ODD2 tracks (23 tracks total).
- (3) Inner Guard Band 1 (IGB1)
 Inner Guard Band 1 is located between IGB2 and Cylinder 0, and is used for speed control during RTZ or Initial Seek sequence. IGB1 consists of four EVEN1—EVEN2 tracks, four ODD1—EVEN2 tracks, four ODD1—ODD2 tracks and four EVEN1—ODD2 tracks (16 tracks total).
- (4) Servo Band
 - Servo Band is used for tracking to determine the center of each cylinder. The Servo Band consists of 148 EVEN1—EVEN2 tracks, 148 ODD1—EVEN2 tracks, 148 ODD1—ODD2 tracks, and 148 EVEN1—ODD2 tracks (592 track total). However, 1-½ inner tracks of Cylinder 0 and 1-½ outer tracks of Cylinder 588 are not utilized for corresponding data tracks.
- (5) Other Guard Band (OGB)
 - The Other Guard Band is used to recognize that the head has passed through the servo zone in an outward direction. OGB consists of four EVEN1—EVEN2 tracks, three ODD1—EVEN2 tracks, three ODD1—ODD2 tracks and four EVEN1—ODD2 track minimum (14 tracks minimum total).

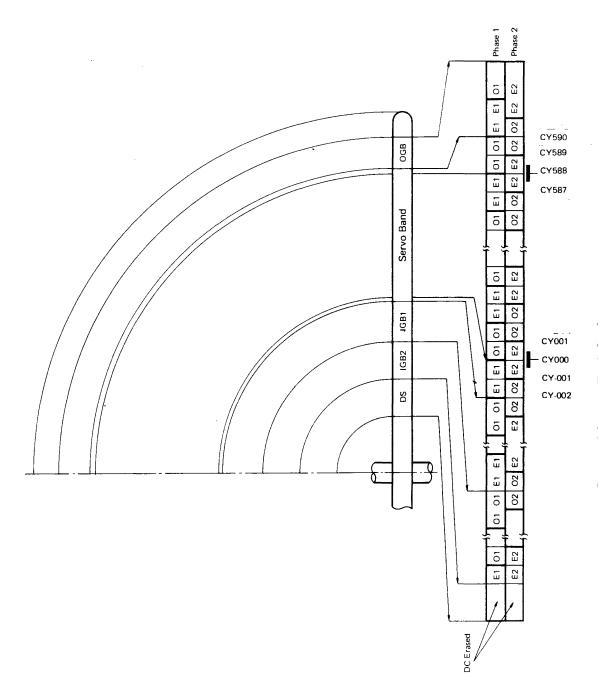


Figure 4-3-3 Servo Track Configuration

4.3.3.2 Servo pattern

The servo signal is a unique "Dual-phase composite servo signal" which creates a high-performance positioning system. It is used to achieve angular positioning (location with reference to the circumference of the disk) and radial positioning (location with reference to the radius of the disk).

Angular positioning is determined by a series of sync bits which are written on each track. Through a combination of Index Bit and Normal Bit; the "sync pattern" is developed. A series of unique sync patterns is written at the factory and used in the identification of specific disk regions. Refer to Figure 4-3-4 and Figure 4-3-5. Index mark, OGB, IGB1, and IGB2 patterns are described in paragraph 4.3.3.3.

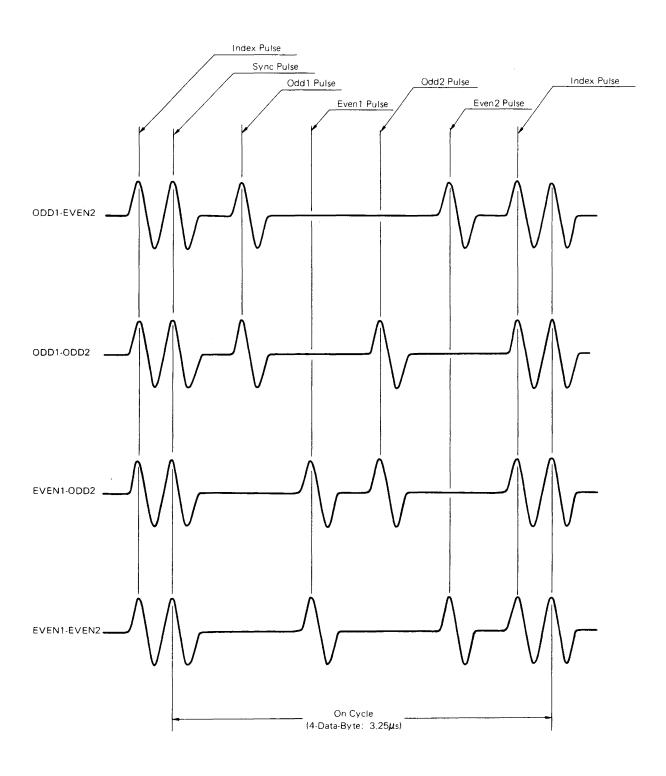


Figure 4-3-4 Normal Bit Pattern

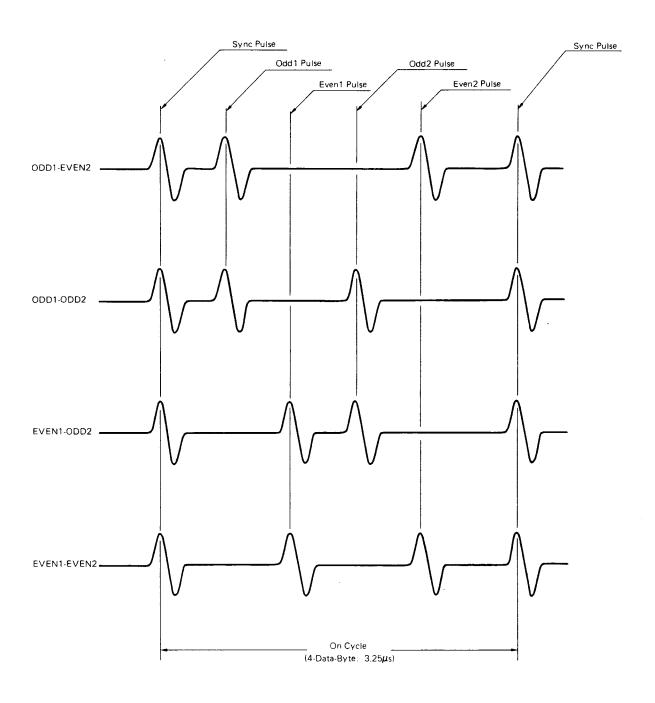


Figure 4-3-5 Index Bit Pattern

Radial positioning information is provided by writing ODD1—EVEN2, ODD1—ODD2, EVEN1—ODD2, and EVEN1—EVEN2 patterns, in that order, on the servo surface.

During head movement, the servo circuit detects the amplitude changes between ODD1 and EVEN1 peaks (phase 1), and between ODD2 and EVEN2 peaks (phase 2), and then converts them into two position signals (phase 1: Normal, phase 2: Quadruture) through the position sensing.

After head movement, the servo head, which has double the core width of the data head, settles on the border of two types of servo patterns controlled by the two least-significant bits of the target cylinder address. The servo circuit then makes the ODD1 (or ODD2) peak equal to the EVEN1 (or EVEN 2) peak by positioning the servo head on the center of the servo track. Refer to Figure 4-3-6.

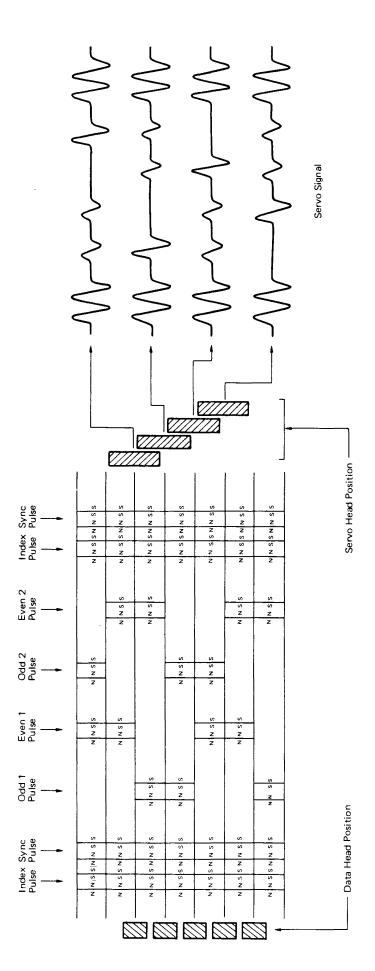


Figure 4-3-6 Dual-Phase Composite Servo Signal

4-12

4.3.3.3 Index, IGB2, IGB1 and OGB patterns

Index, IGB2, IGB1, and OGB patterns are detected by decoding the combination of Index bits and Normal bits. Each of the patterns are shown in Table 4-3-1.

Table 4-3-1 Index, IGB2, IGB1, and OGB Patterns

Signal	Pattern	Pattern interval	
Index	01011	20,480 B (5,120-sync)	
IGB2	01110	256 B (64-sync)	
IGB1	01010	256 B (64-sync)	
OGB	10011	256 B (64-sync)	

Note: 0 - Normal bit

1 — Missing bit

4.3.4 Data Surface Format

The data surface consists of all the disk surfaces except the servo surface and is composed of three basic parts as follows:

(1) Landing Zone (LZ)

The Landing Zone is included in the area described as Behind Home (BH), but is specifically the area the heads contact during start and stop sequence. The Landing Zone corresponds to Dead Space (DS) on the servo surface.

(2) Behind Home (BH)

Behind Home (BH) is the transition area on both sides of the data tracks. It corresponds to IGB2, IGB1, or OGB on the servo surface.

(3) Data Track

The data track area consists of 589 cylinders for data recording, with Cylinder 0 being the inner-most track and Cylinder 588 being the outer-most track.

4.3.5 Head and Surface Configuration

The head and surface configuration for the M2311K and M2312K are given in Figures 4-3-7 and 4-3-8, respectively.

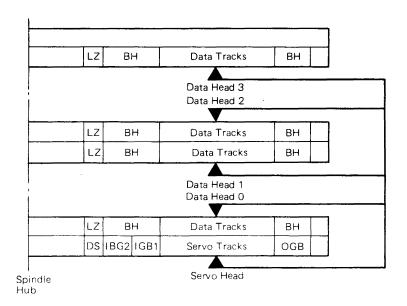


Figure 4-3-7 M2311 Surface Configuration

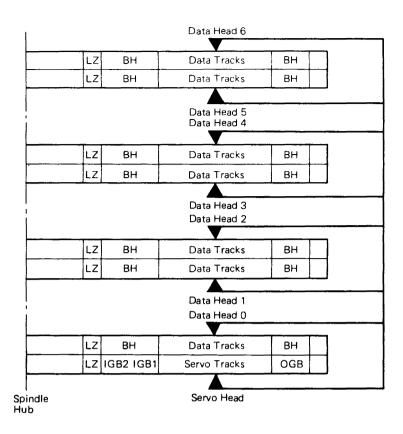


Figure 4-3-8 M2312 Surface Configuration

4.4 FORMAT

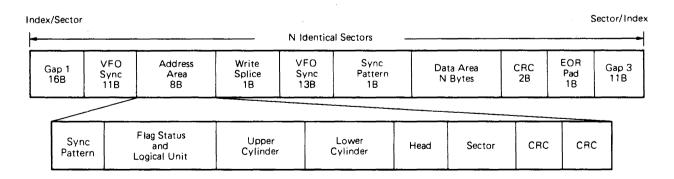
4.4.1 Description

A "sector" is an area assigned an address on the disk. Each sector consists of an Address Area (AA) to confirm that the correct sector has been read, and a Data Area (DA) on which the actual data is recorded.

Index and sector pulses are used by the controller to find the beginning of the track and sector. Sector format is determined by the controller. Fixed Sector format or Variable Sector format can be used with the M231XK.

The recommended Fixed Sector format an Variable Sector format is as follows.

4.4.2 Fixed Sector Format Refer to Figure 4-4-1.



Data Area =
$$\frac{\text{Total Bytes/Track}}{\text{Sector/Track}}$$
 - (Gap loss + Check Bytes)
= $\frac{20480}{64}$ - 64 = 256 Bytes/Sector

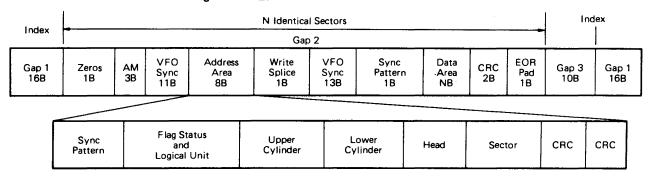
Track Efficiency =
$$\frac{256 \times 64}{20480}$$
 x 100 = 80%

- Notes: 1) This format is an example only and may be structured to suit individual requirements.
 - 2) Sync Byte patterns for address and data areas may be different. It is recommended that Sync Byte patterns are $OE_{(Hex)}$ for address areas and $O9_{(Hex)}$ for data areas.
 - 3) Data patterns for Gap 1, PLO sync, Write Splice, EOR Pad and Gap 3 are all "0".
 - 4) Fixed sectors per track may be any number from 1 through 128 and can be selected by setting the configurator switches on the PCB assembly.

Figure 4-4-1 Fixed Sector Format

4.4.3 Variable Sector Format

Refer to Figure 4-4-2.



Data Area =
$$\frac{\text{Total Bytes/Track} - \text{Index Loss}}{\text{Sectors/Track}} - (\text{Sync + Address Area})$$

Example 1: 64 Sectors/Track

Data Area:
$$\frac{20480 - 26}{64}$$
 - 41 = 278 Bytes/Sector

Track Efficiency =
$$\frac{278 \times 64}{20480} \times 100 = 87\%$$

Example 2: 256 Bytes/Sector

Sector Count =
$$\frac{20480 - 26}{256 + 41}$$
 = 68 Sectors/Track

Track Efficiency =
$$\frac{256 \times 68}{20480}$$
 = 85%

Note: This format is an example only and may be structured to suit individual requirements.

Figure 4-4-2 Variable Sector Format

4.4.4 Description of Format Parameters

4.4.4.1 Fixed Sector Format

(1) Gap 1

Gap 1 allows for displacement of the head and circuit tolerances under worst case conditions. This gap must be a minimum of 16 bytes.

(2) VFO Sync

All "0" is are written and used to synchronize the data from the disk and the read/write clock from the disk VFO circuits. This field must be 11 bytes.

(3) Sync Pattern Byte

The Sync pattern byte represents the start of the address area. It's function is the same as that before the data area, but the address area sync and data area sync byte may be different. The recommended patterns is "OE(Hex)".

(4) Flag Status and Logical Unit Byte

Flag status and logical unit indicates the status of the disk on the sector. Normal record, primary record, or secondary record condition may be indicated. The specifications for this field is a function of the control unit.

(5) Upper Cylinder, Lower Cyclinder

Upper/Lower cyclinder indicates the cylinder address of the track.

(6) Head Address

Head address indicates the head address of the track.

(7) Sector Address

Sector address indicates the sector address of the track.

(8) CRC (Cyclic Redundancy Check)

CRC is a check byte used to determine whether the data was read correctly.

(9) Write Splice

When the address and data areas are written separately, write splice is the location of the read/write head transitions.

(10) VFO Sync

All "0" 's are written and used to synchronize the data from the disk and the read/write clock from the disk VFO circuits.

(11) Sync Pattern

Sync pattern indicates the beginning of the data area. The recommended pattern is "09(Hex)". Refer to (3) above.

(12) Data Area

Data area is where data is actually recorded.

(13) CRC

Same as (8) above for the data field.

(14) EOR Pad

EOR pad eliminates the possibility of destroying the end of a record written with a late displacement head.

(15) Gap 3

Gap 3 is a delay allowance for the control unit. It should be written all "0" 's.

4.4.4.2 Variable Sector Format

This format is written in the Variable Sector Mode. Refer to Figure 4-4-2. Address Mark (AM) is written, prior to the Address Area, to indicate the beginning of a sector, and the data field is written in whatever length necessary to accommodate the system. The Address Mark (AM) is a three-byte DC-erase area at the beginning of the sector format.

4.5 INTERFACE

4.5.1 Introduction

4.5.1.1 Purpose

This section describes the logical and physical specifications for signal transfer between the M231XK and the control unit.

4.5.1.2 Application

These specifications are applicable to both the M2311K (48.2 MB storage) and the M2312K (84.4 MB storage).

4.5.1.3 Connection

The external connection (for transmitting and/or receiving interface signals) consists of connectors, "A" and "B" which connect, respectively, to cables "A" and "B". "A" cables may be connected in a daisy-chain configuration. Therefore, a line terminator must be inserted into the "A" connector of the last device. "B" cables are connected in a start configuration. Therefore, the control unit requires "B" cables and connectors to match the number of units to be connected. Refer to Figure 4-5-1.

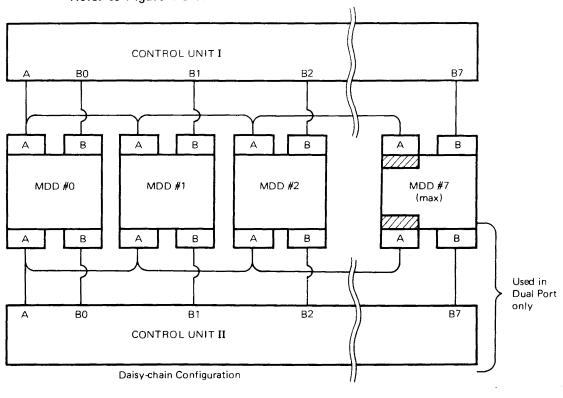
4.5.1.4 Time Specification

Timings are specified at the connector position of the M231XK. Accordingly, it is necessary for signal timings to consider both the delay time of the interface cable and the circuits of the disk control unit.

4.5.1.5 Interface Transmitter/Receiver

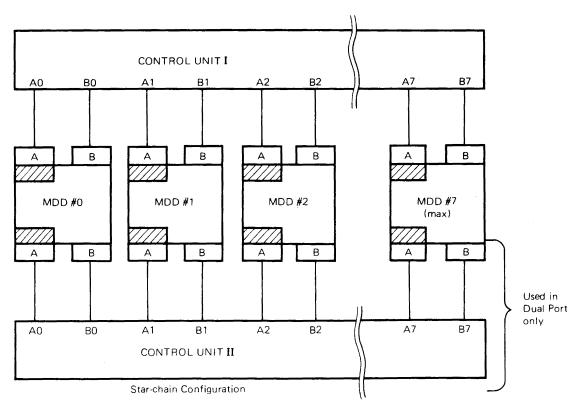
Transmitters and receivers of SN75110 and SN75107 or equivalent are used to provide a terminated, balanced-line transmission system. Refer to Section 4.5.7.1.

4.5.2 Interface Cabling Refer to Figure 4-5-1.



Note: indicates line terminator

a) Daisy-Chain Configuration



b) Star-Chain Configuration

Figure 4-5-1 Interface Cabling

Notes: 1) Line terminators (LTN) are required on the control unit and each unit in a star cable configuration.

2) Line terminators are required on the control unit and last drive in a daisy-chain cable configuration.

Figure 4-5-1 Interface Cabling

4.5.3 Type and Name of Signal Lines

4.5.3.1 "A" Cable Lines for Balanced Transmission Refer to Figure 4-5-2.

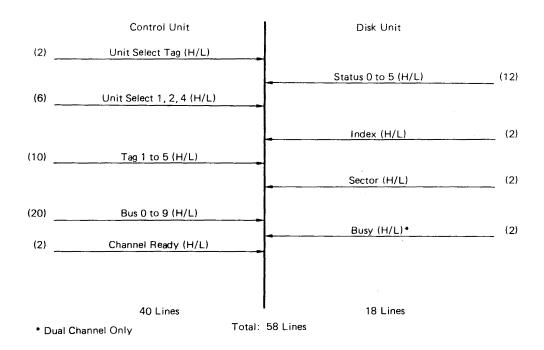


Figure 4-5-2 "A" Cable Signals

4.5.3.2 "B" Cable Lines for Balanced-line Transmission Refer to Figure 4-5-3.

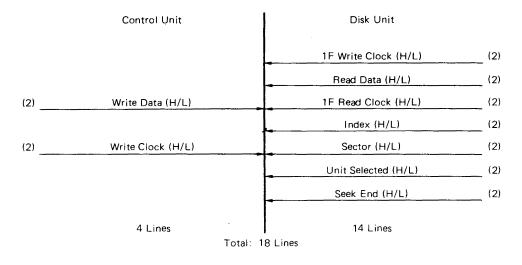


Figure 4-5-3 "B" Cable Signals

4.5.4 Description of Signal Lines

4.5.4.1 "A" Cable Input Signals

(1) Unit Select Tag

This signal gates Unit Select 1, 2, and 4 to select the desired disk. Refer to timing of Unit Select 1, 2, and 4 (Figure 4-5-6).

(2) Unit Select 1, 2, and 4

These three signals are binary-coded to select the desired disk and are validated by the leading edge of Unit Select Tag. The logical disk number (0 through 7) is selectable by means of a switch located on the PCB card.

(3) Tag 1 to 3 and Bus 0 to 9

Refer to Table 4-5-1 which shows the relationship of Tag 1, 2, and 3 and Bus 0 to 9.

Table 4-5-1 Tag/Bus Lines

D	Tag 1	Tag 2	Tag 3	Unit Select Tag *2	
Bus	Cylinder Address	Head Address	Control Select		
0	1	1	Write Gate	_	
1	2	2	Read Gate	_	
2	4	4	Servo Offset Plus	_	
3	8	_	Servo Offset Minus	_	
4	16	-	Fault Clear	_	
5	32	_	AM Enable	_	
6	64	_	RTZ	_	
7	128	-			
8	256	-			
9	512		Release *1	Priority Select	

Note 1: Dual Channel Only.

2: Validates (or gates) the Unit Select 1, 2, and 4 lines in addition to the dual channel priority select line.

(4) Cylinder Address (Tag 1)

Cylinder address is set with Tag 1 and bus lines (Bus 0 to 9) on the 231XK interface. However, throughout Tag 1, the bus lines must be stable. Refer to Figures 4-5-8 and 4-5-9.

The M231XK must indicate On Cylinder Status prior to Tag 1.

(5) Head Address (Tag 2)

The head address is set by Tag 2 and Bus 0 to 3 on the unit. However, throughout Tag 2, Bus 0 to 3 must be stable. Refer to Figure 4-5-10.

Note: Cylinder address and Head address information for the M231XK is shown in Figures 4-5-4 and Figure 4-5-5.

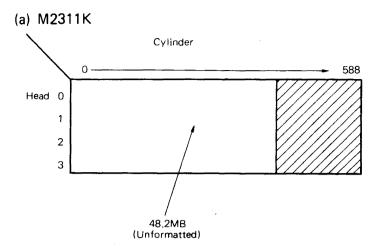


Figure 4-5-4 Storage Addressing M2311K

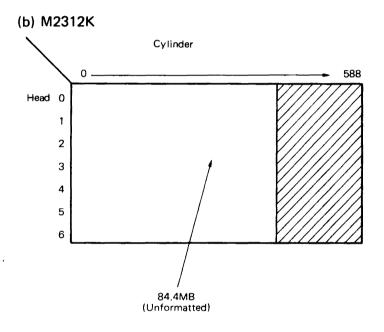


Figure 4-5-5 Storage Addressing M2312K

(6) Control Select

Bus lines 0 to 9 specified by Tag 3 have a different meaning in each bit. All signals are defined as control signals.

(A) Write Gate (Bus 0)

Write Gate signal enables the write operation on the specified track. This signal is validated under the following conditions:

i.	Unit Ready	_	True
ii.	On Cylinder	_	True
iii.	Seek Error	_	False
iv.	Device Check	_	False
v.	Channel Ready	_	True
vi.	File Protect	-	False
víi.	Offset		False

If Write Gate is turned on in cases other than the above-mentioned conditions, Device Check occurs and writing is inhibited. Refer to the definition of a Device Check.

- (B) Read Gate (Bus 1)
 - Read gate signal is used to recover data from the specified track. Refer to the timing of Read Gate, Read Data and 1F Read Clock in Figure 4-5-18 and Figure 4-5-21.
- (C) Servo Offset Plus (Bus 2)

When Servo Offset Plus signal is true on the unit, the head is offset 3.0 μ m from nominal On Cylinder position away from the spindle. Refer to Figure 4-5-11. When going false of Servo Offset Plus, a 4ms delay is required before writing.

- (D) Servo Offset Minus (Bus 3)
 - When Servo Offset Minus signal is true on the unit, the head is offset 3.0 μm from nominal On Cylinder position towards the spindle. Refer to Figure 4-5-11. When going false of Servo Offset Minus, a 4ms delay is required before writing.
- (E) Device Check Clear (Bus 4)

Device check clear signal resets the device check status; however, if any source of a device check still exist (refer to Device Check), this status is not cleard.

(F) AM Enable (Bus 5)

The AM (Address Mark) Enable signal, in conjunction with Write Gate or Read Gate, is used in a variable sector format. When AM Enable is true while Write Gate is ture, an AM of 3-bytes is written on the desired track. When AM Enable is ture while Read Gate is true, the disk read circuit searches an AM of three bytes. When the AM is found, the unit will issue and Address Mark Found signal to the control unit. Refer to Figures 4-5-22 and Figure 4-5-23.

- (G) RTZ (Return to Zero) (Bus 6)
 - No matter where the access heads are located on the media, they are returned to cylinder zero and head zero by the RTZ signal. This signal also clears the Seek Error flip-flop.
- (H) Release (Bus 9) [Dual Channel Only]

The Release command releases Channel Reserve and Unconditionaly Reserve in the drive, making alternate channel access possible after selection by the other channel ceases.

If the customer desires the Release Timer feature using the Release Time switch on the optional Dual Channel PCB assembly, release will occur 500 ms (nominal) after the deselection of the drive. Refer to Figure 4-5-7.

(7) Channel Ready

The Channel ready signal is used to prevent lost of information or damage to the file caused by random interface disturbance when the control unit power is lost. This signal must be stable when the control unit is available, and must be disabled before logic levels decay at the interface lines when a power failure of the control unit occurs. Refer to Figure 4-5-14.

(8) Tag 4 and Tag 5 (selectable)

When Tag 4 goes true, the unit issues Sector Address Status signals on the Status 0 to 5 lines.

When Tag 5 goes true, the unit issues Device Check Status signals on the Status 0 to 5 lines.

When both Tag 4 and Tag 5 are true, the Device Type Code will be issued in BCD on the status 0 to 5 lines. Refer to Table 4-5-2 and Figure 4-5-15.

(9) Pick and Hold

Pick and Hold are not used in M231X Micro Disk Drive.

(10) Priority Select (Dual Channel Only)

When the control unit issues Unit Select Tag and Bus Bit 9 with a specified disk address, the disk drive will be unconditionally selected and absolutely reserved by the channel issuing the command, providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the drive is uncodnitionally reserved by a Priority Select command, the respective channel has exclusive access to the drive. The oppositie channel can access it only after Release command has been issued by the selected channel. Refer to Figure 4-5-7. When a dual port drive is unconditionally reserved, all interface signal are inhibited on the other channel, including unit selected and Busy signals.

4.5.4.2 "A" Cable Output Signals

(1) Status 0 to 5

The status 0 to 5 lines contain status information determined by a combinations of Tag 4 and Tag 5 signals. Information available on status lines 0 to 5 with the various combinators of Tag 4 and 5 signals is specified in Table 4-5-2.

Table 4-5-2 Status Lines Determined by Tag 4/5

Tag 4	False	True	, False	True
Tag 5	False	False	True	True
Status	Unit Status	Sector Address*	Check Status*	Device Type*
0	Unit Ready	Sector Address 1	Control Check 1	Device Type 1
1	On Cylinder	2	2	2
2	Seek Error	4	Read/Write Check 1	4
3	Device Check	8	2	8
4	File Protected	16	3	16
5	AM Found	32	4	32

^{*} Note: These status signals are available if Tag 4/5 function is enabled.

(A) Unit Status

i Unit Ready

When Unit Ready signal is true, and the unit is selected, this signal indicates the unit is up to speed, and no fault condition exists within the unit.

ii On Cylinder

On cylinder line indicates that the heads are located on the specified cylinder (track).

iii Seek Error

Seek Error signal indicates that a seek error has occurred. In this case, the On Cylinder signal does not always go true. The Seek Error is cleared defined as follows:

- a. Seek was unable to complete a move within 500ms.
- b. RTZ was unable to complete a move within 500ms.
- c. The heads have moved to a position outside the recording area.
- d. An illegal cylinder address was issued to the M231XK.
- e. Heads have overshot the new cylinder address.

iv Device Check

Device Check signal indicates that a fault condition exists in the unit. The following fault conditions are detected by the unit.

- a. Control Check 1
 Instructions received during a Not Ready status.
- b. Control Check 2
 Instructions received during a fault condition status. (Write Gate received during an off-set operation, reading or Seek Error condition).
- Read/Write Check 1
 Write Gate received during Off-track status, DC Motor overcurrent, or VCM overcurrent.
- d. Read/Write Check 2

Write fault or write current detected during a not-write operation.

e. Read/Write Check 3

Write Gate received during write protected status.

f. Read/Write Check 4

Write or Read Gate received and multiple heads are selected.

If an above-mentioned condition has occurred, writing is immediately inhibited and a Device Check signal is issued to the control unit. The device check status is cleared by a fault clear on tag 3 and bus 4; or by an active fault clear on the operator panel (if operator panel is employed.)

Device Check Status turns on the check lamp on the operator panel as well as Fault Indicator LEDs on PCB assembly.

v File Protected

File Protected signal indicates that the selected M231XK is in a write-protected status. The File Protect function is enabled by the following switches:

- a. File Protect Switch on the operator panel (option)
- b. File Protect Switch on the PCB assembly.

Attempting to write while protected will cause a Device Check (Read/ Write Check 3) to be issued to the control unit.

vi Address Mark Found

Address Mark Found is an eight-byte pulse which is sent to the control unit at least two bytes after the recognition of three-byte DC-erased area.

(B) Sector Address 1 to 32 (Status Lines 0 to 5)

Six bits of binary-coded Sector Address indicate the current sector address in the unit. They are transferred from the Sector Counter, reset by the trailing edge of Index, and clocked by the trailing edge of Sector. Sector Address (Status Lines 0 to 5) is issued to the control unit by activating Tag 4.

Refer to Figure 4-5-16 for timing of Sector Address (status lines 0 to 5).

(C) Device Check (Status 0 to 5)

Refer to item (A)-iv.

(D) Device Type 1 to 32 (Status lines 0 to 5)

Enabling Tag 4 and Tag 5 lines causes Device Type Status to be issued to the control unit as Status 0 to 5 signals. Binary-coded Device Type signals are specified as show in Table 4-5-3.

Table 4-5-3 Device Type Code

			Status				
Device Type	Decimal Value	0	1	2	3	4	5
		2º	2 ¹	2 ²	2 ³	2 ⁴	2 ⁵
M2311	34	0	1	0	0	0	1
M2312	35	1	1	0	0	0	1

Notes: 0-False; 1-True

(2) Index

The Index signal occurs once per revolution and is used for reference in read/write operation to indicate the beginning of a track.

Refer to Figure 4-5-16 for the timing of Index and Sector.

(3) Sector

The Sector Mark is derived from the servo track. The number of sectors per revolution is switch-selectable and is determined by counting Byte Clock pulses. The switches are located on the VFO/PLO card within the PCB assembly. Each key of SW2 and SW3 represents a binary powers of the Byte Clock count.

(4) Busy (Dual Channel Only)

If the drive is already selected and/or reserved, a Busy signal will be issued to the "A" cable and the Unit Selected signal will be issued to the "B" cable of the channel attempting the select function. The Busy signal will remain until the Unit Select Tag is negated or the drive is no longer busy. Unit Selected signal should be used to enable Busy in the control unit. Refer to Figure 4-5-6.

4.5.4.3 "B" Cable Input Signals

(1) Write Data

Write Data line carries the serial NRZ data to be written on the disk surface Write Data must be synchronized with Write Clock. Refer to Figure 4-5-17.

(2) Write Clock

Write Clock is a return signal of the 1F Write Clock issued from the M231XK; it must be synchronized with the serial NRZ Write Data. Refer to Figure 4-5-17.

4.5.4.4 "B" Cable Output Signals

(1) 1F Write Clock

1F Write Clock signal is used by the control unit to synchronize Write Data and Write Clock. It is available during Unit Ready Status except during read operations. Refer to Figure 4-5-17.

(2) Read Data

Read Data line transmits the recovered data in the form of serial NRZ data synchronized with 1F Read Clock. Refer to Figure 4-5-18.

(3) 1F Read Clock

1F Read Clock defines the beginning of a bit cell. The Read Data is synchronized with the 1F Read Clock. Refer to Figure 4-5-18.

(4) Unit Selected

When the three unit-select lines compare with the logical address of the unit, and when the leading edge of Unit Select Tag is received, the Unit selected Signal goes true and is issued to the control unit. This signal also activates all status lines at the "A" Cable.

(5) Seek End

Seek End signal is a combination of On Cylinder and Seek Error, indicating that a Seek RTZ, or Offset operation has terminated.

In the Dual Port function, the Seek End signal sent to the unselected channel will normally be a constantly true signal level. However, if the drive is selected by one channel, and the other channel receives a select, the Seek End signal sent to the waiting channel will go false for 30 μ s, when the Select and Reserve latches are reset on the selected channel.

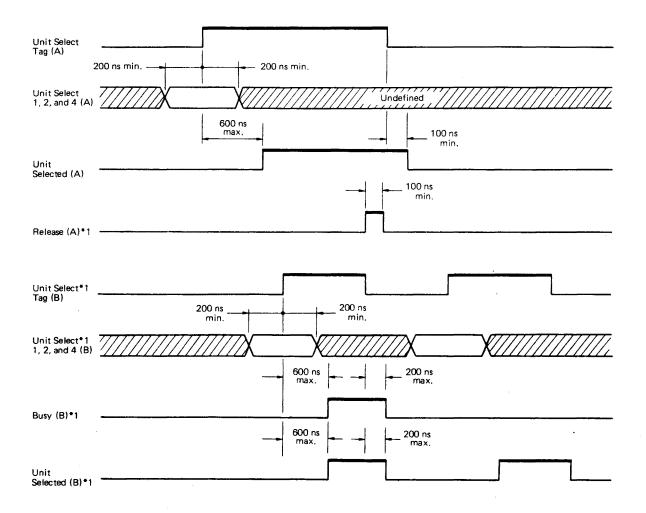
(6) Index, Sector

The Index and Sector pulses are issued on the interface for reference during read/write operations.

4.5.5 Control Timing

4.5.5.1 Unit Selection

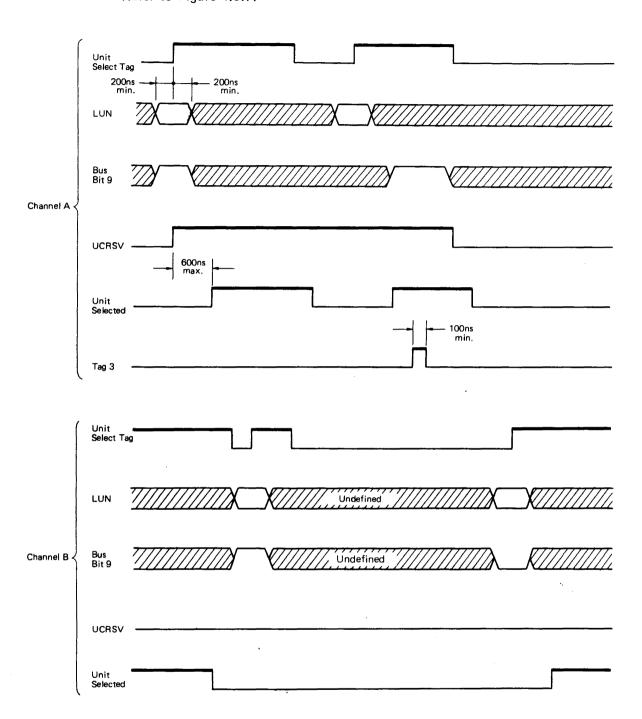
Refer to Figure 4-5-6.



Note: * 1-Dual Channel only.

Figure 4-5-6 Unit Select Timing

4.5.5.2 Priority Select Timing (sample) Refer to Figure 4.5.7.



- Notes: 1) LUN: Logical Unit Number (Unit Select 1, 2 and 4).
 - 2) UCRSV: Unconditionally Reserved (Priority Selected).
 - 3) Sample Sequence is as follows;

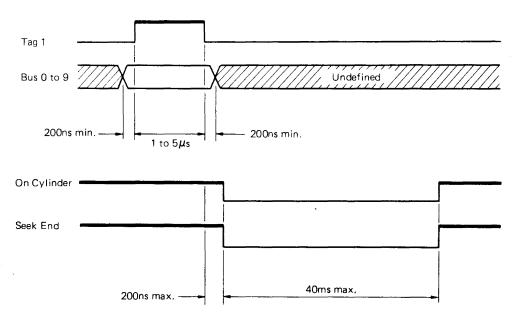
 CHB Selected → CHA Priority Select → CHB Priority Select → CHA Release → CHB Select

Figure 4-5-7 Priority Select Timing

B03P-4590-0103A...B 4-27

4.5.5.3 Direct Seek Timing (Tag 1)

Refer to Figure 4-5-8.



Note: Cylinder Address must be less than 589.

Figure 4-5-8 Direct Seek Timing

4.5.5.4 Zero Track Seek Timing Refer to Figure 4-5-9.

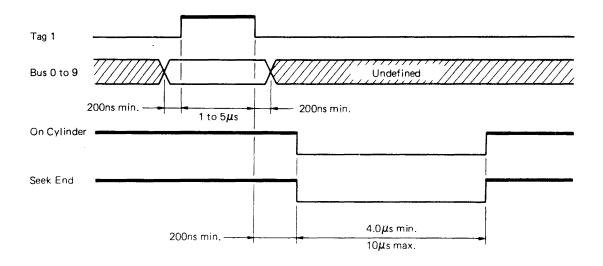


Figure 4-5-9 Zero Track Seek Timing

4.5.5.5 Tag 1 to Tag 2 Timing Refer to Figure 4-5-10.

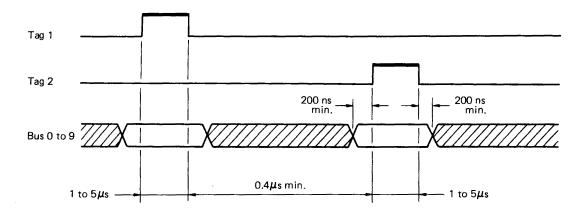


Figure 4-5-10 Tag 1 to Tag 2 Timing

4.5.5.6 Offset Timing

Refer to Figure 4-5-11.

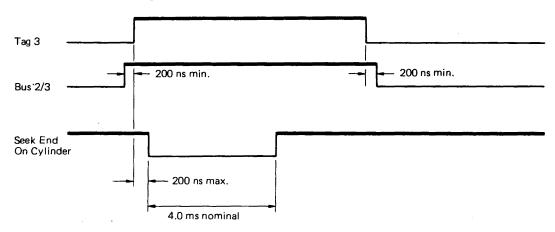


Figure 4-5-11 Offset Plus/Minus Timing

4.5.5.7 Device Check (Fault) Clear Timing Refer to Figure 4-5-12.

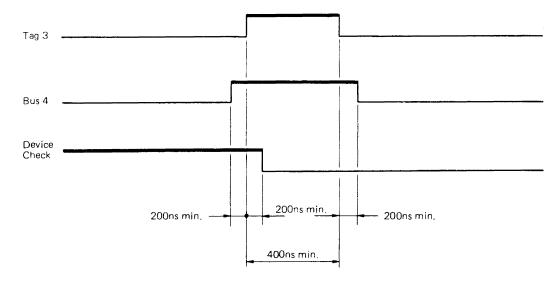


Figure 4-5-12 Fault Clear Timing

4.5.5.8 RTZ Timing Refer to Figure 4-5-13.

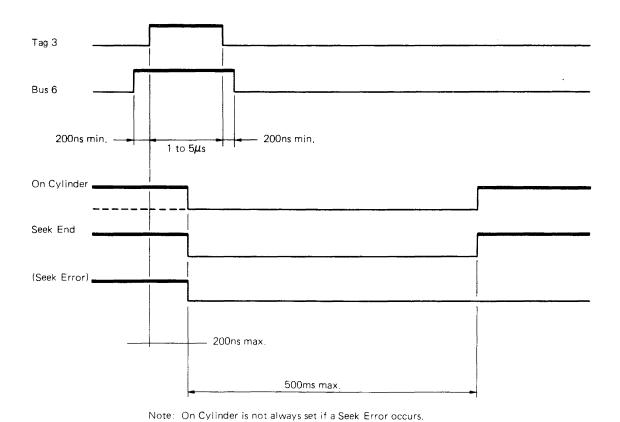


Figure 4-5-13 RTZ Timing

4.5.5.9 Channel Ready Timing Refer to Figure 4-5-14.

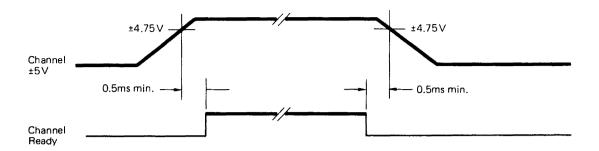


Figure 4-5-14 Channel Ready Timing

4.5.5.10 Tag 4/5 and Status 0 to 5 (optional) Timing Refer to Figure 4.5.15.

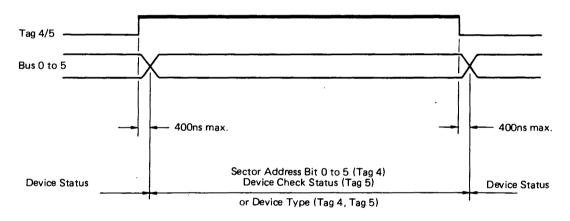


Figure 4-5-15 Tag 4/5 Timing

B03P-4590-0103A...A

4-31

4.5.5.11 Index/Sector Timing Refer to Figure 4-5-16.

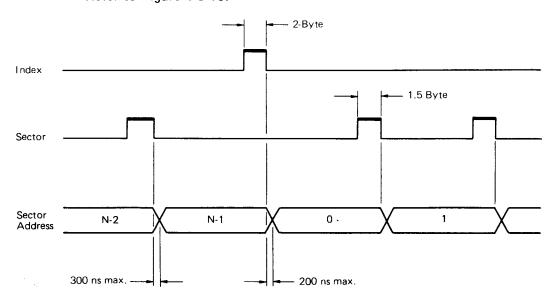
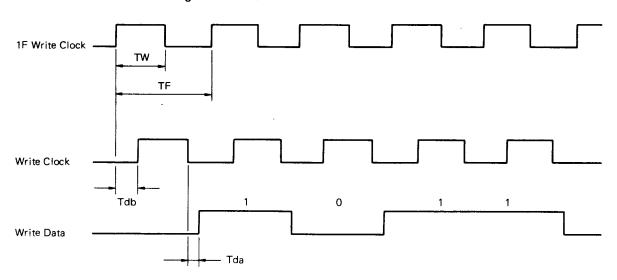


Figure 4-5-16 Index and Sector Timing

4.5.5.12 1F Write Clock, Write Data/Write Clock Timing Refer to Figure 4-5-17.



Tw = TF/2

TF = 101.7 ns ± 2 ns

Tdb = Continuous delay within 2 bits

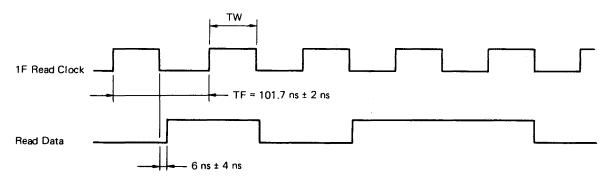
Tda = 0 ± 10ns

- Notes: 1. Write Data and Write Clock timing shall be specified at the output connector of the control unit.
 - 2. The permissible value of TF=101.7ns ± 2ns is about 2%, which includes the rotational speed tolerance, 1% and the servo jitter, ±1%.
 - 3. NRZ Write Data issued from the control unit is write-compensated and then MFM-modulated for writing on the disk surface.

Figure 4-5-17 Write Data and Write Clock Timing

4.5.5.13 Read Clock/Read Data Timing

Refer to Figure 4-5-18.



Tw = TF/2

- Notes: 1. 1F Read Clock and Read Data timing shall be specified at the output connector of the disk unit.
 - Read Data signal should be clocked at the positive-going edge of 1F Read Clock on the control unit.

Figure 4-5-18 1F Read Clock and Read Data Timing

4.5.6 Read/Write Timing

4.5.6.1 Format Write

Refer to Figure 4-5-19.

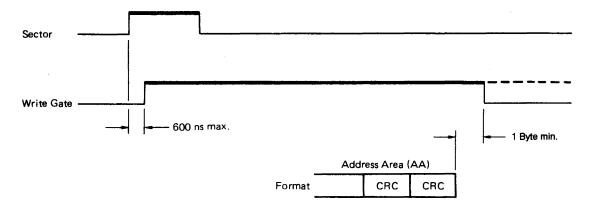


Figure 4-5-19 Format Write Timing

4.5.6.2 Data Write

Refer to Figure 4-5-20.

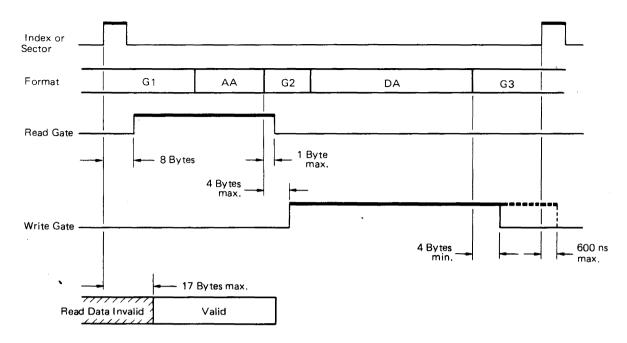
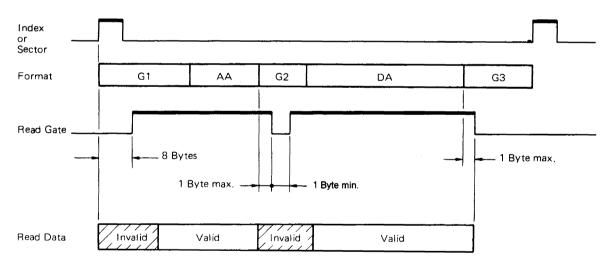


Figure 4-5-20 Write Data Timing

4.5.6.3 Data Read

Refer to Figure 4-5-21.



- Notes: 1. The invalid data in the above figure is inhibited in the unit; therefore, it may be disregarded in the control unit.
 - 2. The timing for switching to 1F Read Clock should be performed after the invalid data. In this case, a phase adjustment is required for 1 or 2 bits.

Figure 4-5-21 Read Data Timing

4.5.6.4 AM Write (Variable Soft Sector Only) Refer to Figure 4-5-22.

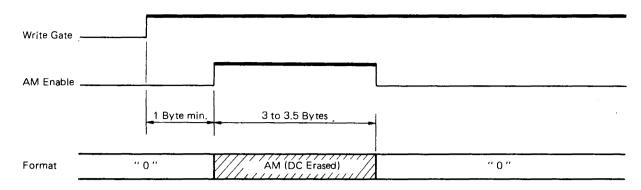


Figure 4-5-22 AM Write Timing

4.5.6.5 AM Read (Variable Soft Sector Only) Refer to Figure 5-5-23.

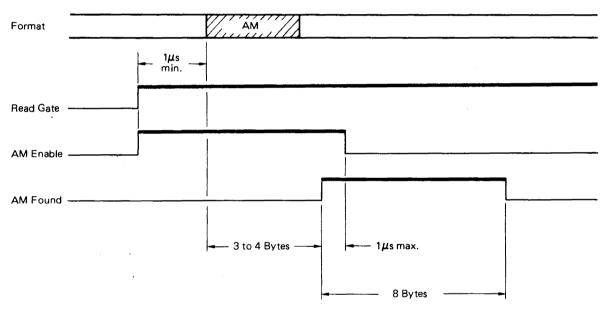


Figure 4-5-23 AM Read Timing

4.5.6.6 Write-To-Read Recovery Time

Refer to Figure 4-5-24. When head selection has been stabilized, the recovery time before Read Gate can be enabled after Write Gate goes false is 10 μ s minimum.

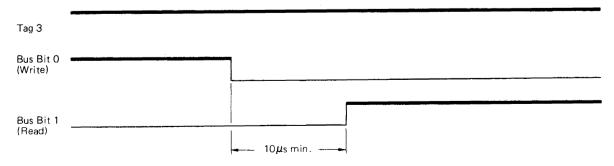


Figure 4-5-24 Write-To-Read Recovery Time

4.5.6.7 Head Select Transient

Refer to Figure 4-5-25. There is a 5 μ s delay within the disk drive due to circuit characteristics between the deselection of one head and the selection of another head.

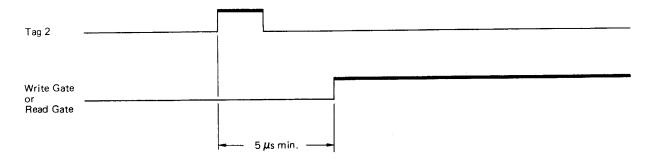
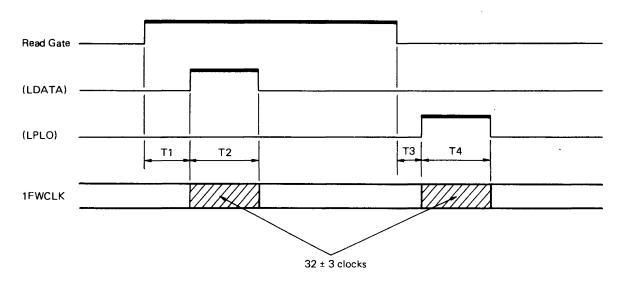


Figure 4-5-25 Head Select Transient

4.5.6.8 1F Write Clock in Reading

In the read operation, the 1F Write Clock signal fluctuates slightly within the Lock-To-Data or Lock-To-PLO signal (internal signal of Variable Frequency Oscillator circuit), in shown as Figure 4-5-26.



T1:-30 to 35 bits; T2/T4:-32 bits (4 Bytes); T3:-2 to 11 bits.

Figure 4-5-26 1F Write Clock in Reading

4.5.7 Interface Transmission

4.5.7.1 Driver and Receiver

Transmitters and receivers of SN75110 and SN75107 or equivalent are used to provide a terminated, balanced-line transmission. The Driver is SN75110 or equivalent, and the Receiver is SN75107/SN75108 or equivalent.

(1) Driver

Refer to Figure 4-5-27 and Table 4-5-4.

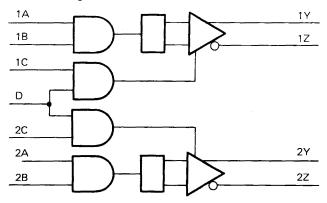


Figure 4-5-27 Drive Logic Diagram (SN75110)

Table 4-5-4 SN75110 Function Table

Logic Inputs		Inhibit Input		Outpu	ıts
Α	В	С	D	Υ	Z
Х	Х	L	Х	OFF	OFF
X	Х	Х	L	OFF	OFF
L	X	Н	Н	ON	OFF
х	L	Н	Н	ON	OFF
Н	H	Н	Н	OFF	ON

Note: H-High Level, L-Low Level, X-Irrelevant.

(2) Receiver

Refer to Figure 4-5-28 and Table 4-5-5.

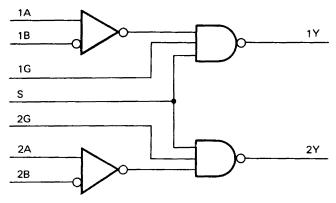


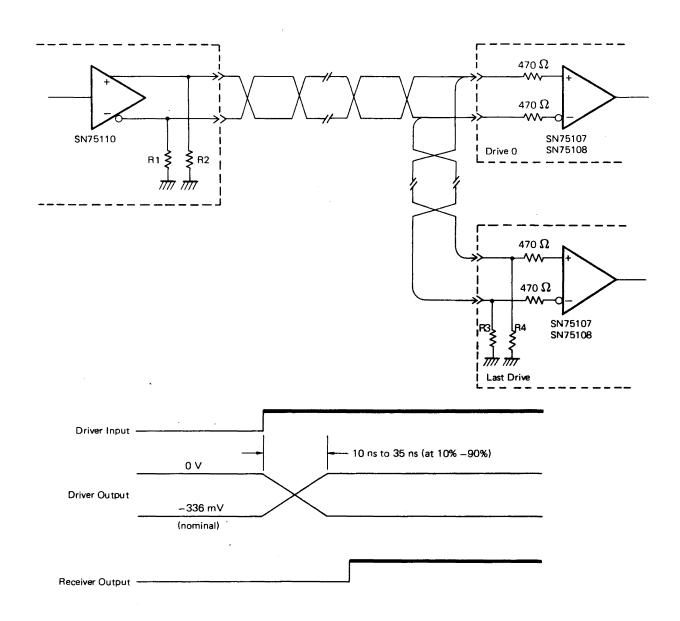
Figure 4-5-28 Receiver Logic Diagram (SN75107/75108)

Table 4-5-5 SN75107/75108 Function Table

Differential Immute	Stro	bes	Output
Differential Inputs	G	S	Y
A−B ≥ 25 mV	Х	х	н
	х	L	Н
–25 mV <a−b <25="" mv<="" td=""><td>L</td><td>X</td><td>Н</td></a−b>	L	X	Н
	Н	Н	Indeterminate
	Х	L	Н
A−B ≤ −25 mV	L	X	Н
	Н	Н	L

Note: $H-High\ Level; L-Low\ Level; X-Irrelevant.$

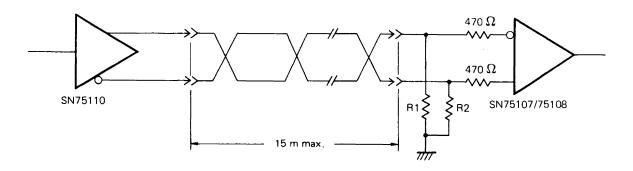
4.5.7.2 "A" Cable (Control Cable) Transmission Refer to Figure 4-5-29.

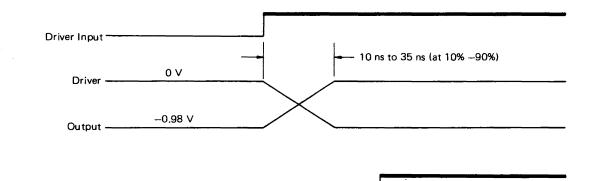


- Notes: 1. Line terminators are located on the unit and the controller. R1 to R4: 56 Ω ± 5 %, 1/10W.
 - 2. A line terminator is located on the terminator assembly of the last unit in the daisy chain configuration.
 - 3. The maximum cable length is 30 meters.

Figure 4-5-29 Balanced Transmission of "A" Cable

4.5.7.3 "B" Cable (Data Cable) Transmission Refer to Figure 4-5-30.



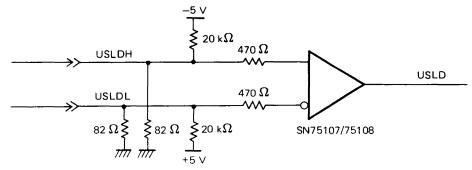


a) Balanced Transmission of "B" cable

Receiver Output

Note: 1. Cable shall be flat with characteristic impedance of 100 ± 10 ohms.

- Line terminators are located on the receivers at the drive or control unit. R1 and R2 are 82 ohms ± 5%, 1/10W.
- 3. The protect resistors (470 ohms) should be located on the receiver side. 470 Ω ± 5 %, 1/10W.
- 4. A bias network should be used to prevent disturbance conditions by power failure at the control unit end of Unit Selected and Seek End signals as in b).



b) Bias Network to Prevent Power Future Disturb

Figure 4-5-30 Balanced Transmission "B" Cable

4.5.7.4 Channel Ready Driver

The Channel Ready signal must be issued so that data is protected during a power failure of the control unit. Relay logic and passive terminations sometimes aid this requirement. If SN75110A drivers are used to drive the Channel Ready signal from the control unit, dual drivers should be connected in parallel, and no 56 ohm termination to ground should be used at the control unit.

4.5.8 Connectors and Cables

4.5.8.1 Connectors

(1) "A" Cable connectors (60 positions) Refer to Table 4-5-6.

Table 4-5-6 "A" Cable Connectors

Connector	Fujitsu Specification				
Drive Side	FCN-702P060-AU/M FCN-704P060-AU/M FCN-705P060-AU/M	(Wire Wrapping) (Straight) (Right Angle)			
Cable Side	FCN-707J060-AU/B FCN-707J060-AU/O	(Closed End) (Through End)			

(2) "B" Cable connectors (26 positions) Refer to Table 4-5-7.

Table 4-5-7 "B" Cable Connectors

Connector	Fujitsu Specification				
Drive Side	FCN-702P026-AU/M FCN-704P026-AU/M FCN-705P026-AU/M	(Wire Wrapping) (Straight) (Right Angle)			
Cable Side	FCN-707J026-AU/B FCN-707J026-AU/O	(Closed End) (Through End)			

4.5.8.2 Cable

Refer to Table 4-5-8.

Table 4-5-8 Cable

Cable	Specification		
А	455-248-60 Spectra Strip Zo = 100 ohms ± 10 ohms 28 AWG, 7 strands		
В	174-26 Ansley / 3476-26 3M Zo = 100 ohms ± 10 ohms / Zo = 130 ohms ± 15 ohms 28 AWG, 7 strands / 28 AWG, 7 strands		

4.5.9 Connector Pin Assignment

4.5.9.1 "A" Cable Connector 60 Pin

Refer to Table 4-5-9.

Table 4-5-9 "A" Cable Pin Assignment

Pin	Function	Pin	Function
1	Tag 1 L	31	Tag 1 H
2	Tag 2 L	32	Tag 2 H
3	Tag 3 L	33	Тад 3 Н
4	Bus 0 L	34	Bus 0 H
5	Bus 1 L	35	Bus 1 H
6	Bus 2 L	36	Bus 2 H
7	Bus 3 L	37	Bus 3 H
8	Bus 4 L	38	Bus 4 H
9	Bus 5 L	39	Bus 5 H
10	Bus 6 L	40	Bus 6 H
11	Bus 7 L	41	Bus 7 H
12	Bus 8 L	42	Bus 8 H
13	Bus 9 L	43	Bus 9 H
14	Channel 1 Ready L	44	Channel Ready H
15	Status 3 L	45	Status 3 H
16	Status 2 L	46	Status 2 H
17	Status 1 L	47	Status 1 H
18	Index L	48	Index H
19	Status O L	49	Status O H
20	Status 5 L	50	Status 5 H
21	Busy L (Dual Channel Only)	51	Busy H (Dual Channel Only)
22	Unit Select Tag L	52	Unit Select Tag H
23	Unit Select 1 L	53	Unit Select 1 H
24	Unit Select 2 L	54	Unit Select 2 H
25	Sector L	55	Sector H `
26	Unit Select 4 L	56	Unit Select 4 H
27	Tag 5 L (Selectable)	57	Tag 5 H (Selectable)
28	Status 4 L	58	* Status 4 H
29	(Pick): Not used	59	(Hold): Not used
30	Tag 4 L (Selectable)	60	Tag 4 H (Selectable)

4.5.9.2 "B" Cable Connector 26 Pin

Refer to Table 4-5-10.

Table 4-5-10 "B" Cable Pin Assignment

Pin	Function	Pin	Function
1	GND	14	1F Write Clock H
2	1F Write Clock L	15	GND
3	Read Data L	16	Read Data H
4	GND	17	1F Read Clock H
5	1F Read Clock L	18	GND
6	Write Clock L	19	Write Clock H
7	GND	20	Write Data H
8	Write Data L	21	GND
9	Unit Selected H	22	Unit Selected L
10	Seek End L	23	Seek End H
11	GND	24	Index H
12	Index L	25	GND
13	Sector L	26	Sector H

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4.6 ELECTRICAL CIRCUIT FUNCTION

4.6.1 Start/Stop Control

A block diagram of Start/Stop Control is shown in Figure 4-6-1. DC power of +5 V, -12 V and +24 V is applied to the drive from the power supply unit or the system power. The +12 V required for the servo circuit is regulated from +24 V on TUZM PCB assembly. The -5.2 V required for VFO circuit is regulated from the -12 V on CNAM PCB assembly.

The DC voltage Monitor circuit (which monitors +5 V, -12 V, +24 V, and +12 V) issues a Power Ready (PWRDY) signal when these voltages are within the specified range. When +5 V DC is supplied to the drive, the Crystal Oscillator circuit issues a 15,728,640 Hz clock signal, (which is divided by eight and converted into Control Clock 1 (CTCL1) of 1,966,080 Hz frequency.

The leading edge of PWRDY signal sets the Accelerate DC Motor (ACDM) signal which accelerate the DC Motor, and simultaneously connect the DC Motor windings with the DC Motor control circuit by driving the Relay 1 (RL1). The DC Motor is accelerated according to the phase of the Speed Sensor outputs (three Hall-effect elements), which is then converted into a Set Speed (STSPD) signal once per revolution. When the rotational speed is up to 3,366 rpm (±6%), Speed Good (SPGD) is issued, and it resets the seek control logic.

When the DC Motor is further accelerated (up to 3,600 rpm), the DC Motor Control circuit changes to inertia mode from accelerate mode; simultaneously a Start Pulse (STARTP) signal is issued, which initiates the initial seek sequence. The completion of initial seek sequence sets unit Ready status to the control unit. The rotational speed is monitored once per revolution, and accelerate mode and inertia mode are repeated to maintain the rotational speed at its nominal value of 3,600 rpm ± 2%.

The stop sequence is triggered by a DC power failure of +5 V, -12 V, +24 V, or internal +12 V, by turning off the PWRDY signal. When the PWRDY signal is reset, the DC Motor winding is separated from the power amplifier and connected with the Brake resistors through the contacts of RL1. Disk rotation will completely stop 40 seconds after the power failure.

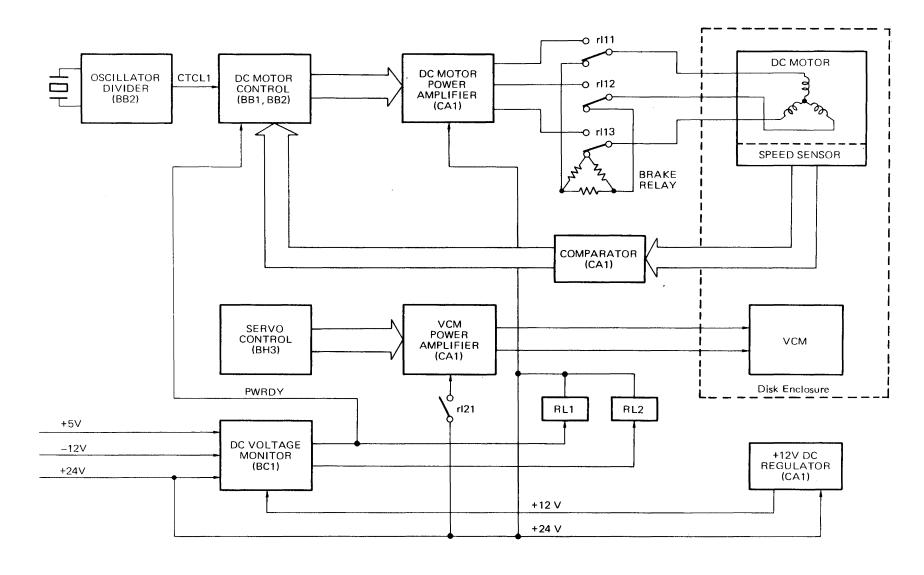


Figure 4-6-1 Start/Stop Control Block Diagram

4.6.2 DC Motor Control

The block diagram of DC Motor Control is shown in Figure 4-6-2.

As mentioned in Section 4.6.1 (Start/Stop Control), the leading edge of PWRDY signal initiates the acceleration of the DC Motor according to the phase outputs of the Speed Sensor. During the start-up sequence, the Current Limiter limits the winding-flow current to 4.2A nominal by detecting the voltage level at the bleeder resistor.

The Crystal Oscillator generates a 15,728,640 Hz clock signal, which is divided into the 1,966,080 Hz Control Clock 1 (CTCL1) signal to control the DC Motor.

When the spindle rotation is initiated by initial stage, the Speed Sensor output is converted into TTL level signals (Phase A, B and C: PHA, PHB and PHC), are then applied to Speed Detect and DC Motor Fault Detect circuits. The PHA, PHB, and PHC signals have two cycles per revolution.

The positive-going edge of PHA signal sets the next latch and the negative-going edge of *PHB signal resets this latch; the latch output signal is then applied to the Clock Synchronize and Divider circuits which generate Set Speed (STSPD) and Timer Clock (TMCLK) signals once per revolution. The TMCLK signal resets the Divide Counter at the leading edge, and is also applied to the Time-out Counter. The STSPD signal is applied to the Speed Detect and Accelerate Latch circuits.

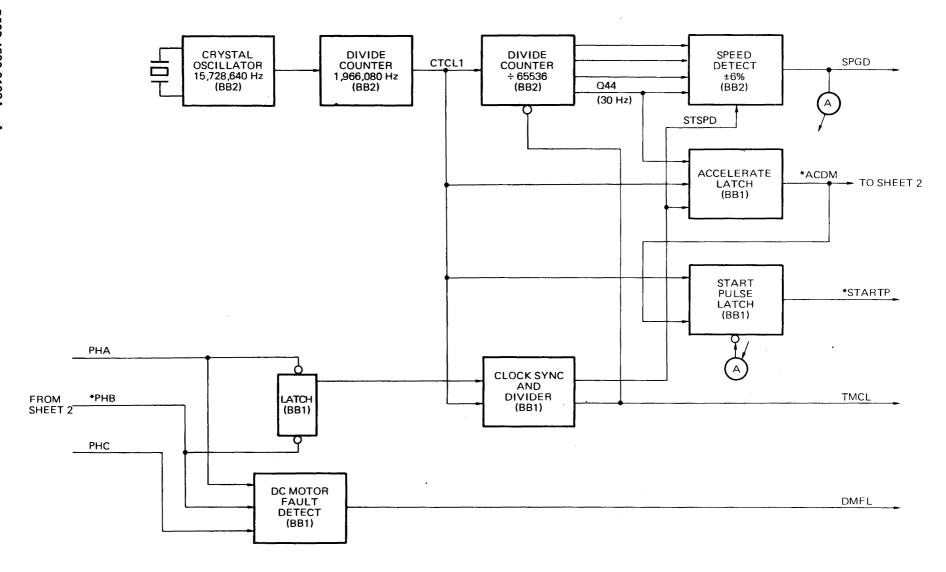


Figure 4-6-2 DC Motor Control Block Diagram (Sheet 1 of 2)

Figure 4-6-2 DC Motor Control Block Diagram (Sheet 2 of 2)

During the power-up sequence, the leading edge of PWRDY signal sets the Q44 signal which is final stage output of the Divide Counter (Divided by 65536). The Q44 signal inhibits the count-up function of the Divide Counter until the counter is reset by the leading edge of the TMCLK signal, and also is clocked by the leading edge of the STSPD signal. When the Q44 signal goes true, this indicates that the rotational speed is slower than nominal speed. When the rotational speed is within $\pm 6\%$ of nominal speed, the Speed Good (SPGD) signal goes true.

Twenty seconds after power on, when the Q44 signal is false at the leading edge of the STSPD signal, DC Motor control mode is changed to inertial mode from accelerate mode. Simultaneously, the STARTP signal, which starts the initial seek sequence, is issued at the first negative going-edge of the ACDM signal. The DC Motor control then repeats the accelerate mode and inertia mode and maintains the rotational speed at 3,600 rpm ±2%.

The timing chart of the DC Motor power-up sequence is shown in Figure 4-6-3.

In accelerate mode, the ACDM signal is set by the leading edge of the STSPD and the Q44 signal at the PHA, *PHB and PHC signals are the decoded into binary signals. By combining of these decoder outputs, the power amplifier drives the DC Motor windings as shown in Figure 4-6.4.

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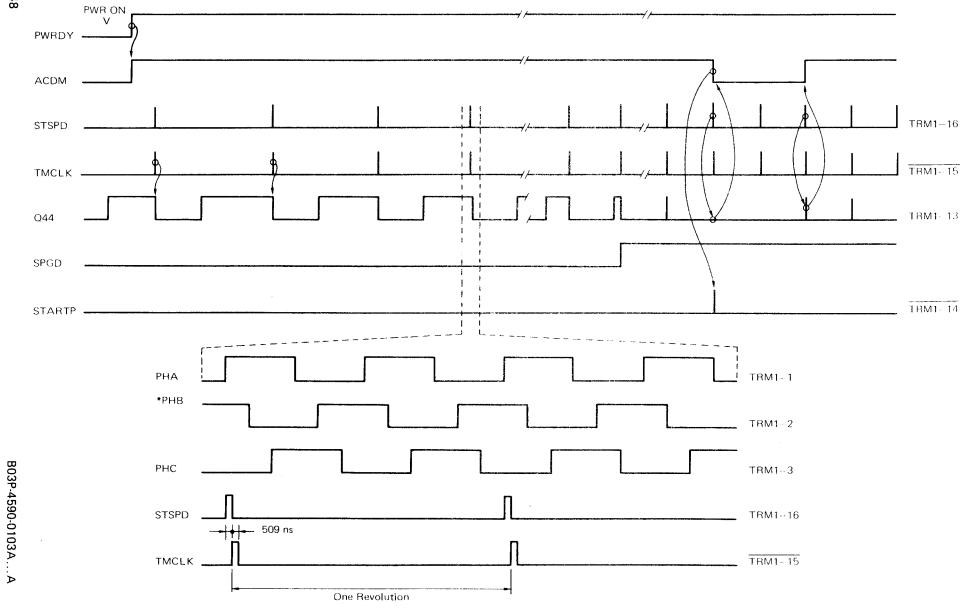
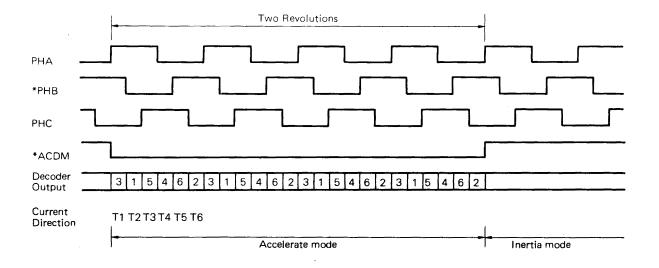


Figure 4-6-3 Power Up DC Motor Control



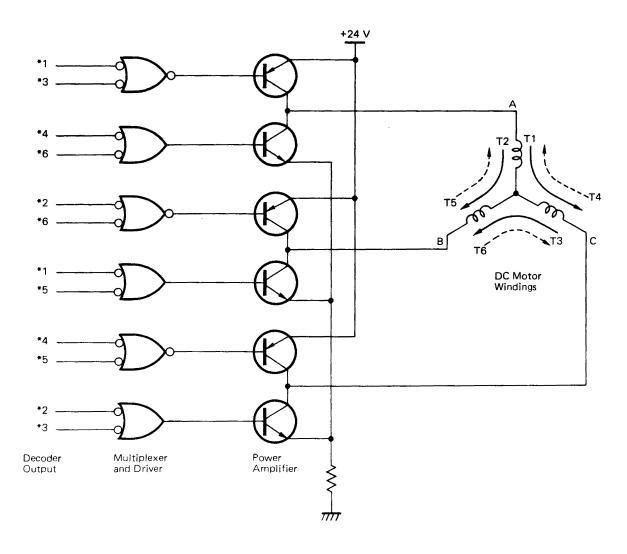


Figure 4-6-4 DC Motor Accelerate/Inertia Mode Control

4.6.3 Unit Selection

The Micro Disk Drive must be selected before it will respond to any commands from the control unit. Tag and Bus receivers are not enabled until the unit is selected.

This describes the dual channel functions releated to selection. They are as follows:

- Unit address select
- Reserve
- Release
- Priority select (unconditional reserve)
- Disable with a maintenance switch
 The functional block diagram of dual port is shown in Figure 4-6-5.

4.6.3.1 Unit Address Select and Reserve

A unit is selected or reserved in an identical sequence which is initiated by Unit Select Tag (USLTG) and a unit address signal (Unit select 1, 2, 4: USL 1, 2, 4). However, this sequence cannot start when:

- The unit is selected and reserved by the opposite channel.
- The unit is not selected, but reserved by the opposite channel.
- The channel which has attempted to select the unit is disabled by the maintenance switch on the unit or because the unit is placed in the Priority Select state by the opposite channel.

The select/reserve sequence is as follows:

Suppose that the unit is ready to be selected that is, any of the above three condition does not exist. A controller sends USLTG and USL 1, 2, 4 to the unit. If the unit address from the channel-A controller agrees with the logical unit number (LUN), the unit sends Unit Selected to the channel-A controller through cable B when Channel-A Compare (CHACMP) is sent to the XCDM printed circuit board. This sequence is the same as with the single-port configuration.

Unless the unit is selected or reserved by channel-B and, as a result, is Busy, CHACMP causes the Channel A Selected signal (CHASLD) to be sent in synchronization with Clock 1 (CLK1) from the oscillator. CHASLD turns on the Channel-A Enable (CHAENB) signal to make the driver/receiver for Channel-A ready for transmission/reception, drive the LED to indicate CHASLD, switch the WDAT/WCLK multiplexer to Channel-A, set Busy to indicate that the unit is selected or reserved by the Channel-A controller, and trigger the Set Reserve (STRSV) one-shot multivibrator to set the reserve latch.

If channel-A and B attempt to select a unit at the same time, CLK1 and CLK2 (clocks with the same frequency and different phases) determine which channel is to access the unit. As a result, Busy is set.

The STRSV one-shot multivibrator output sets the Channel A Reserved (CHARSV) latch about 300 ns after CHASLD. This CHARSV signal turns on the LED on the XCDM printed circuit board, sets BUSY A, and sets Seek End B (SKENDB) to "1" before its transmission to Channel-B. SKEND to Channel-B is kept "1" as long as the unit is reserved by Channel-A.

The unit is kept selected/reserved by Channel-A until Channel-A is disabled by the maintenance switch or until USLTG becomes false. When Channel-B attempts to select the unit, the unit sends BUSYA as a busy signal to Channel-B, and sends also Unit Selected B (USLDB) to indicate that it is selected/reserved by Channel-A.

Even when USLTG from Channel-A goes false after the select/reserve sequence, the unit remains reserved by Channel-A. This reserved state is not reset until a Release command comes from Channel-A, Channel-A is disabled by the main-

tenance switch, Channel-B performs Priority Select, or the power is turned on/off.

If the opposite channel control unit attempts to select own channel while it is selected or reserved by the own channel control unit (i.e. in Busy state), Tried Latch in the dual channel is set. Thus, at the time when the own channel becomes neither selected nor reserved, Seek End goes flase for $30\mu s$ so that the opposite channel having been waiting can be indicated an interrupt.

If the unit is in Disabled state (realized by Priority Select from the opposite channel or by Disable switch) and own channel attempts to select the unit, no signal response is activated.

The block diagram of the select/reserve circuit is shown in Figure 4-6-6, and the related flowchart and timing chart are shown in Figures 4-6-7 and 4-6-8, respectively.

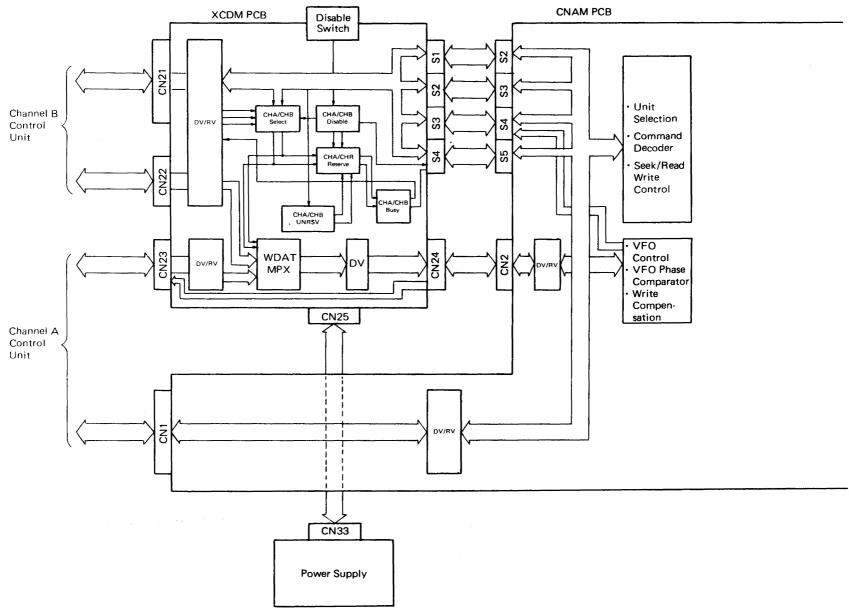


Figure 4-6-5 Functional Block Diagram of Dual Channel

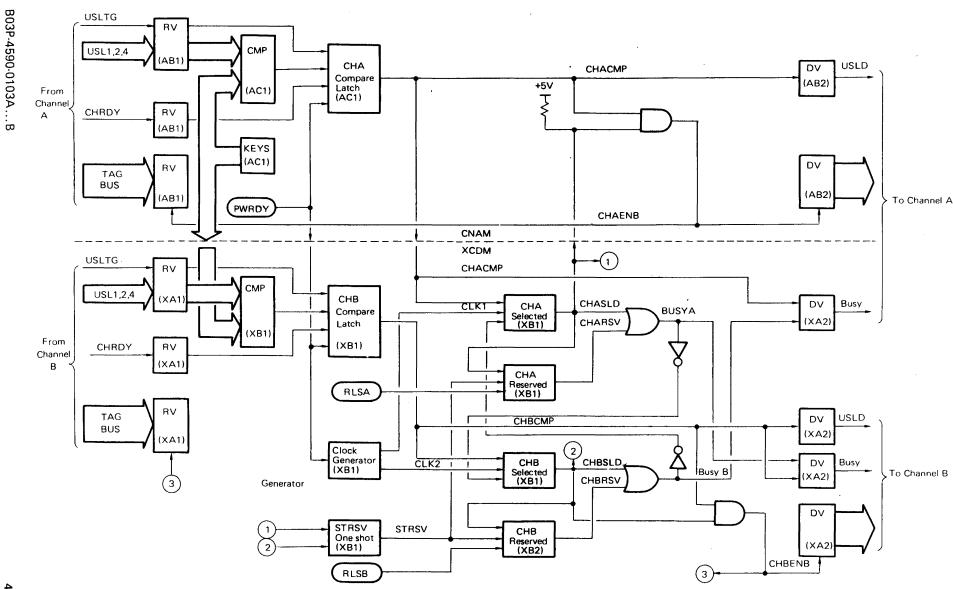


Figure 4-6-6 Functional Block Diagram of Select/Reserve

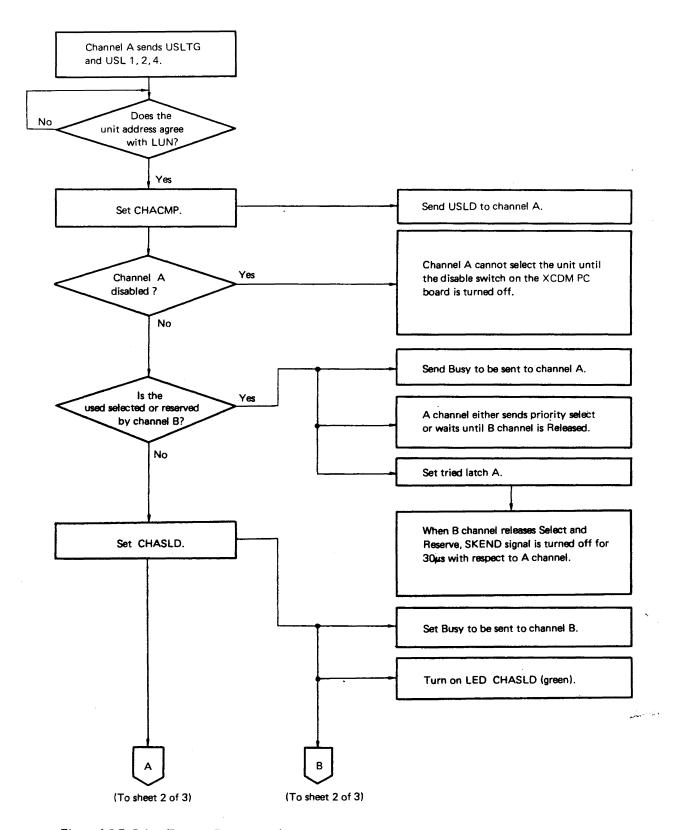


Figure 4-6-7 Select/Reserve Flow Chart (Sheet 1 of 3)

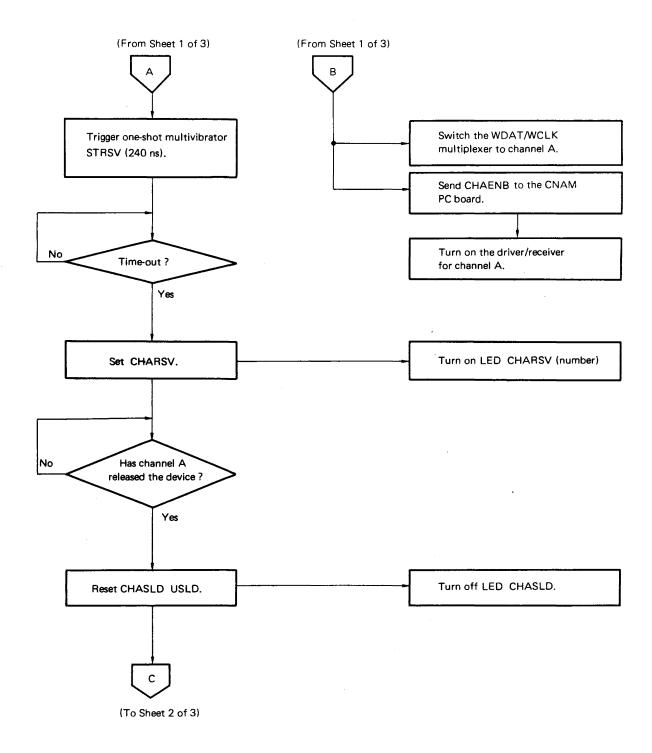


Figure 4-6-7 Select/Reserve Flow Chart (Sheet 2 of 3)

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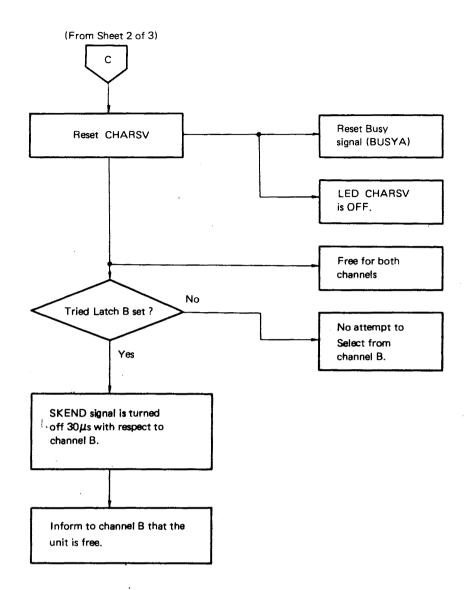


Figure 4-6-7 Select/Reserve Flow Chart (Sheet 3 of 3)

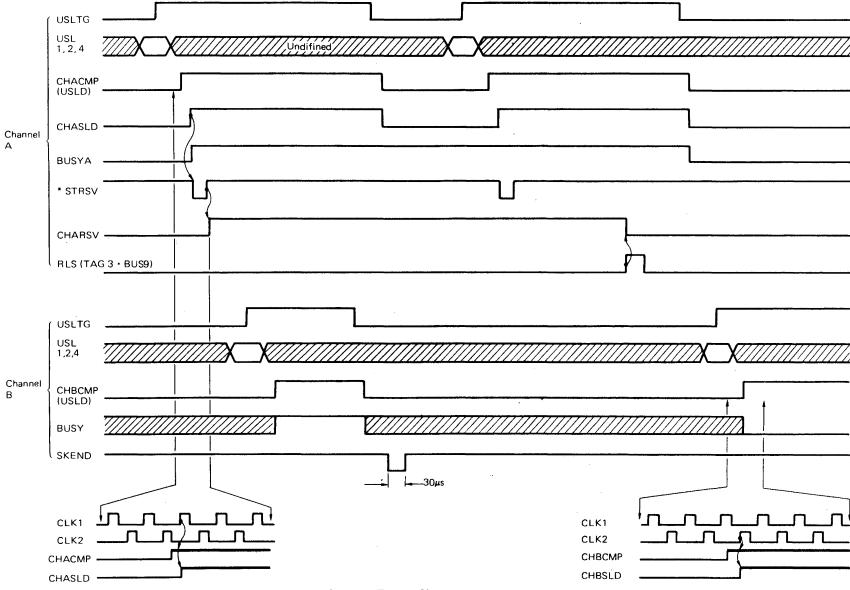


Figure 4-6-8 Select/Reserve Timing Chart

4.6.3.2 Release

The release command resets the reserved and priority select (unconditional reserve) states. Release is executed by two functions described in the following. One is a release command from a control unit (Tag 3 Bus bit 9) and the other is Release Timer of the dual channel option.

(1) Release command (Tag 3, Bus bit 9)
Reserve and Priority Select (unconditional reserve) are reset by the leading edge of Tag 3 and Bus Bit 9 sent from the control unit. Thus, it is made possible to be accessed from the control unit of the opposite channel.

(2) Release Timer

If the switch on the dual channel is set to the RLTM position. The Release function is enabled by the unit itself. If unit Select Tag signal goes false when the switch is being set at the RLTM position, the Release Timer one-shot of 500 ms is triggered. The Reserve Latch is reset by the trailing edge of the Release Pulse.

If the switch is set to ABSL (Absolute Reserve) side, the one-shot is disabled.

4.6.3.3 Priority Select (Unconditional Reserve)

Even if a unit is selected or reserved (except unconditional reserve) by a channel, the opposite channel can switch the unit to this channel by issuing a Priority Select (Unit Select Tag, unit address and Bus Bit 9) command.

The command sets the Unconditionally Reserved (UCRSV) latch to inhibit all signals, Select/Reserve is given to the channel and, at the same time, the channel which was previously connected is disconnected. Once it is set in an unconditional reserve state, all signals are disabled for respect to the opposite channel.

The Unconditionally Reserve is released only by the release command given by the channel exclusively connected.

4.6.3.4 Disable Switch

During maintenance the interface functions released to channels A and B can be inhibited by using the maintenance switch on the XCDM printed circuit board. This disable function can be done for the two channels separately.

4.6.4 Seek Control Logic Function

The MDD M231XK has four types of seek modes: Initial Seek, Return To Zero (RTZ), Direct Seek by Tag 1, and Linear Mode.

(1) Initial Seek Mode

The Initial Seek Mode positions the heads at Cylinder 0 during power-up sequence.

(2) Return To Zero Mode

The Return To Zero (RTZ) mode moves the heads to Cylinder 0, regardless of where they are when the RTZ command is received. Return To Zero mode is essentially equivalent to the Initial Seek mode; therefore, they are both referred to as the Go To Zero (GTZ) mode.

(3) Direct Seek Mode

The Direct Seek mode causes a seek to the cylinder address specified by Bus bit 0 to 9, Tag 1 signals from the control unit.

(4) Linear Mode

Linear mode causes the heads to track the center of the specified cylinder after any of the afore-mentioned seek operations has been completed. An Offset operation is available in the Linear mode.

When a power failure or seek malfunction has occurred on the unit, each seek mode is reset and the heads are returned to the Landing Zone by the retract spring in the actuator assembly.

The Seek Control Logic block diagram is shown in Figure 4-6-9.

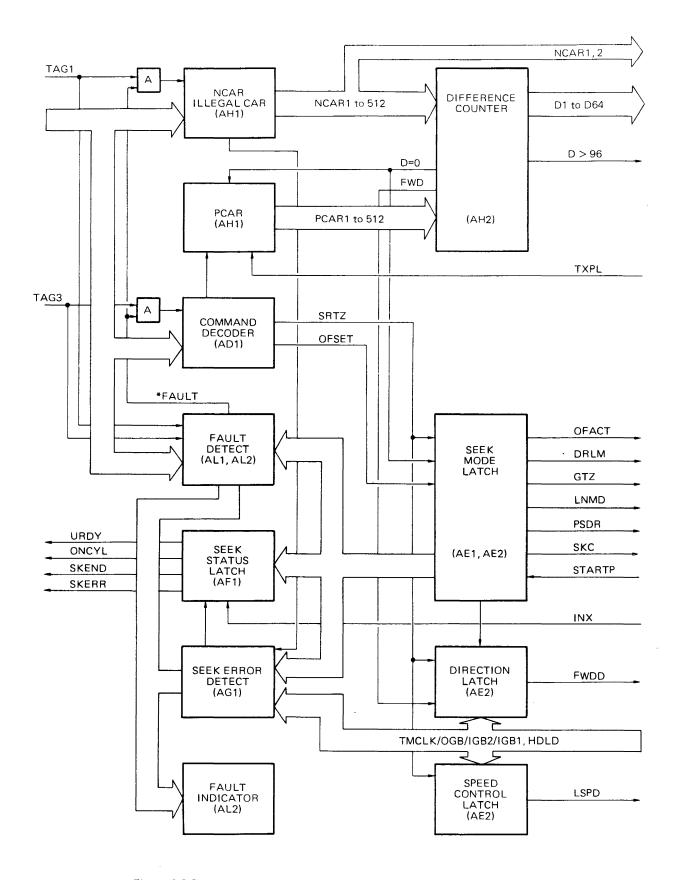


Figure 4-6-9 Seek Control Logic Block Diagram

4.6.4.1 Initial Seek Mode

The Start Pulse (STARTP) is issued to the Seek Control circuit when the spindle rotational speed has reached its nominal value. The STARTP signal sets Initial Seek Mode (INSKM), Go To Zero Mode (GTZM), Under Sequence (UNSQ), Drive Linear Motor (DRLM), and Forward Drive (FWDD) latches, and resets the Low Speed (LSPD) latch.

At the start of Initial Seek, the heads move toward the outside of the disk (forward) at high speed by enabling FWDD and disabling Low Speed (LSPD).

When the heads have passed through the IGB2 zone and enter the IGB1 zone, the heads are driven toward the outside of the disk at low speed by enabling the FWDD and LSPD signals.

When the heads have passed through IGB1 zone, the Position Drive (PSDR) goes true, which changes the target velocity to the Position signal. When the velocity reaches the capture range, V=0 signal goes true which then resets the DRLM and PSDR lathes and set the Linear Mode (LNMD) latch. When the LNMD signal goes true, it keeps the heads precisely on the center of Cylinder 0, that is, the first ODD1—EVEN1 and EVEN1—EVEN2 servo track.

The first Index signal under the linear mode triggers the Settling 1 one-shot (STL1:2.5 ms). The trailing edge of the STL1 signal sets the Seek End (SKEND), On Cylinder (ONCYL), and Unit Ready (URDY) latches, and also resets the INSKM, GTZM, and UNSQ latches.

If the initial seek has not been performed within 500 ms after STARTP, the Device Check goes true, Not Ready status is ture. The Device Check Clear signal, under the not ready status, which is commanded from the control unit or the Check Clear key, will cause a retry of the Initial Seek sequence.

The Return To Zero (RTZ) command, with a complete servo-off sequence and during the Ready status, initiates the Initial Seek sequence.

The Go To Zero flow chart is shown in Figure 4-6-10, and the timing chart for Initial Seek is shown in Figure 4-6-11.

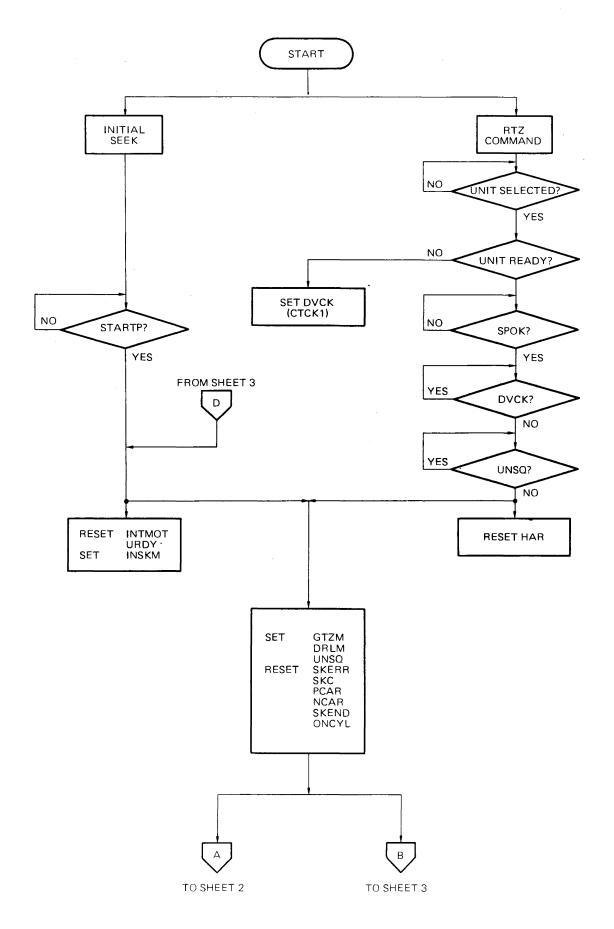


Figure 4-6-10 Go To Zero Flow Chart (Sheet 1 of 3)

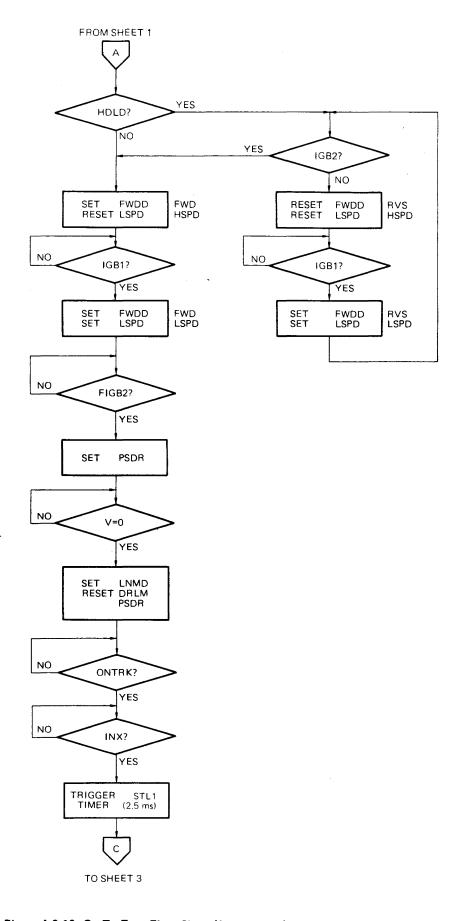


Figure 4-6-10 Go To Zero Flow Chart (Sheet 2 of 3)

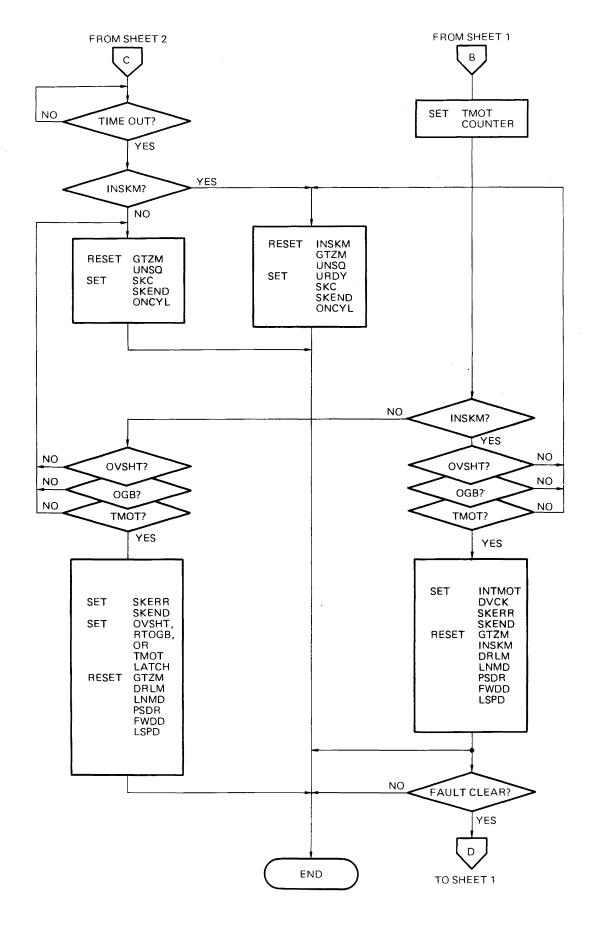


Figure 4-6-10 Go To Zero Flow Chart (Sheet 3 of 3)

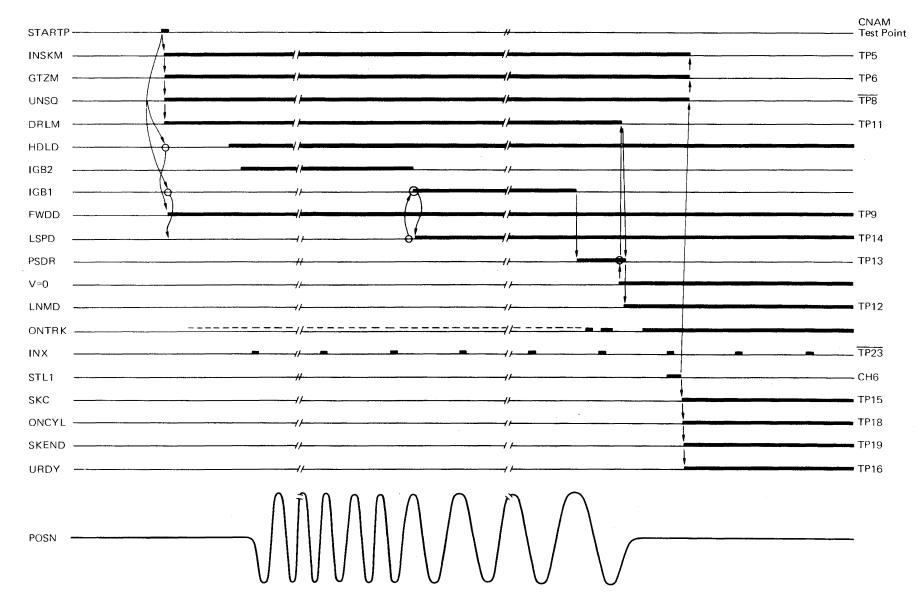


Figure 4-6-11 Initial Seek Timing Chart

4.6.4.2 Return To Zero Mode

The Return To Zero mode is initiated by a Return To Zero (RTZ) command from the control unit during Ready status and linear mode.

The RTZ command sets GTZM, DRLM, and UNSQ latches; resets SKEND, ONCYL, and Seek Error (SKERR) latches; and resets Present Cylinder Address Register (PCAR), Next Cylinder Address Register (NCAR), and Head Address Register (HAR).

At the start of GTZM, the heads move toward the center of the disk (reverse) at high speed by disabling the FWDD and LSPD signals.

When the heads have passed through the Servo Zone and enter the IGB1 zone, they are driven toward the center of the disk at low speed.

When the heads enter the IGB2 zone, they are driven toward the perimeter forward) at high speed. Upon entering the IGB1 zone again, they are driven forward at low speed.

The subsequent sequence is equivalent to the Initial Seek Mode.

The RTZ timing chart is shown in Figure 4-6-12.

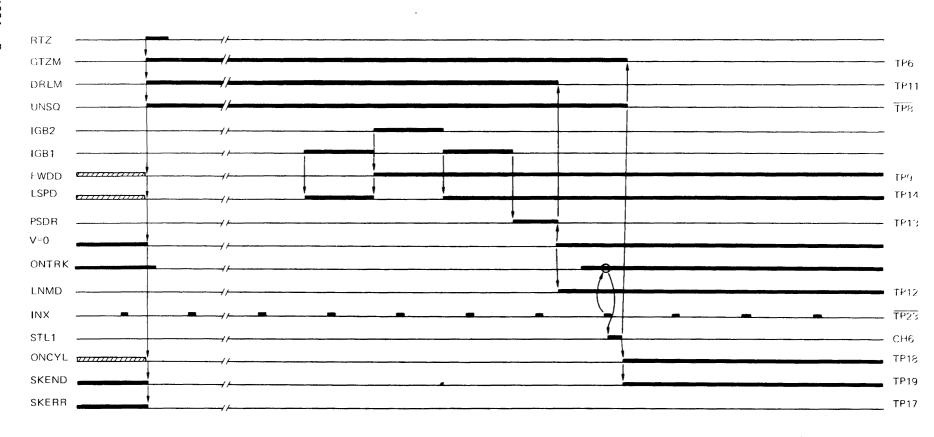


Figure 4-6-12 Return To Zero Timing Chart

4.6.4.3 Direct Seek Mode

Direct Seek mode is initiated by activating the Tag 1 signal.

The leading edge of Tag 1 sets the bus bits 0 to 9 into the Next Cylinder Address Register (NCAR) when the bus contains an address of less than 588.

When the NCAR output is not equal to the Present Cylinder Address Register (PCAR) output at the trailing edge of the Tag 1 signal (Fall Tag 1 = FTAG1), a Direct Seek is initiated.

The FTAG1 signal resets the ONCYL, SKEND, LNMD, and V=0 latches, and also sets the SEKM, DRLM, UNSQ, and direction latches.

NCAR1 and 2 signals are applied to the Servo Control circuit to determine the phase of target cylinder.

The difference between NCAR and PCAR is equal to the number of cylinders to be moved to the desired address. The difference counter output binary-coded D1 to D64 and D > 96, is sent to the servo control circuit to generate the target velocity.

When the NCAR is greater than PCAR, the forward direction is set, and when the NCAR is less than the PCAR, the reverse direction is set using the FWDD signal.

When the heads start to move to the desired address, the Track Crossing Pulse (TXPL) is sent from the servo circuit to the PCAR counter every time the servo head crosses a cylinder. The PCAR counter is increased by the trailing edge of the TXPL signal in the forward direction, and is decreased in the reverse direction.

When the difference is equal to zero, the Position Drive (PSDR) signal is activated and the velocity follows the position signal. When the V=0 signal goes true, LNMD latch is set, and DRLM and PSDR latches are reset. The successive ONTR signal triggers the Settling 1 (STL1) one-shot (2.5 ms). The trailing edge of STL1 signal sets the ONCYL and SKEND latches and reset the SEKM and UNSQ latches.

If NCAR is equal to PCAR at the leading edge of Tag 1, a No Motion Seek (NOSEK) signal is activated and triggers Settling 2 (STL2: 5μ s) one-shot. The ONCYL and SKEND signals are reset by the trailing edge of the TAG1 signal and then ONCYL and SKEND signals go true at the trailing edge of STL2 signal.

If an illegal cylinder address (CAR > 588) is issued from the control unit, the trailing edge of the TAG1 signal resets the ONCYL and SKEND signals and then sets the Seek Error (SKERR) and SKEND signals immediately. The LNMD latch is also reset as the heads move to the Landing Zone.

The Direct Seek flow chart is shown in Figure 4-6-13 and the timing chart is shown in Figure 4-6-14.

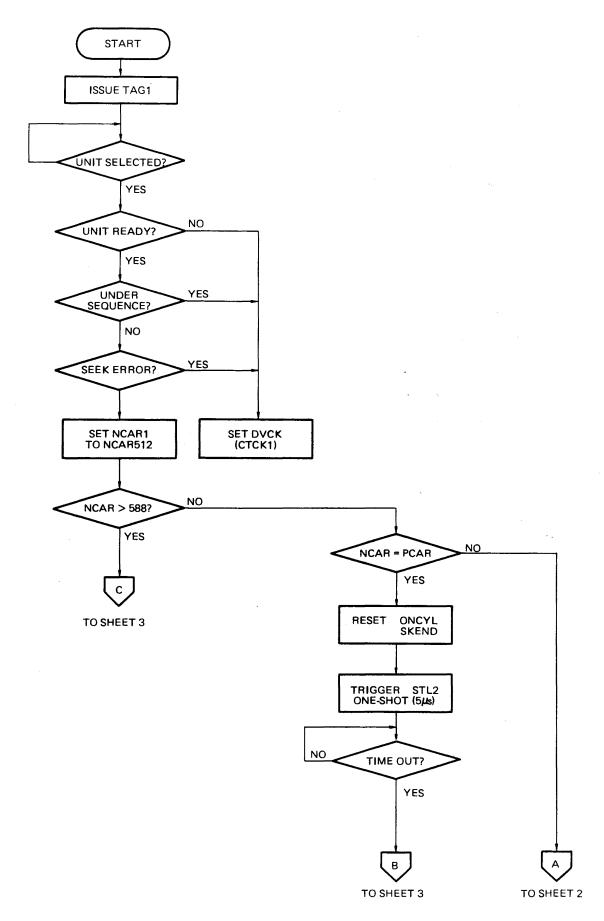


Figure 4-6-13 Direct Seek Flow Chart (Sheet 1 of 3)

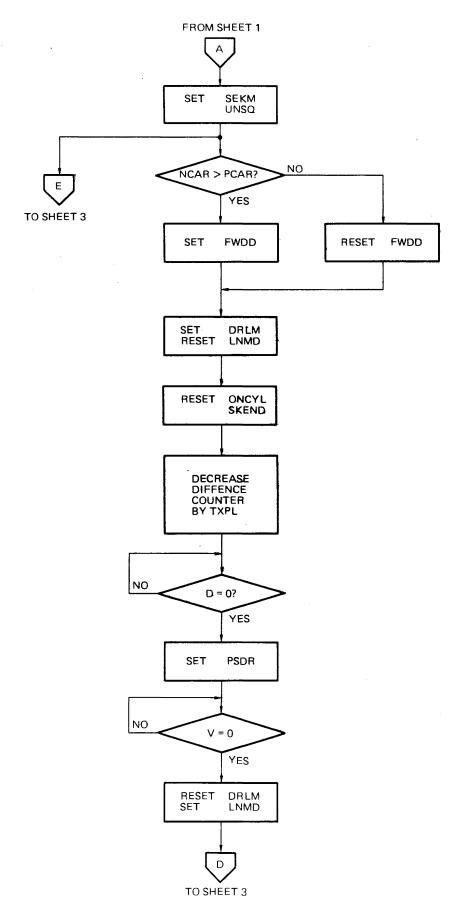


Figure 4-6-13 Direct Seek Flow Chart (Sheet 2 of 3)

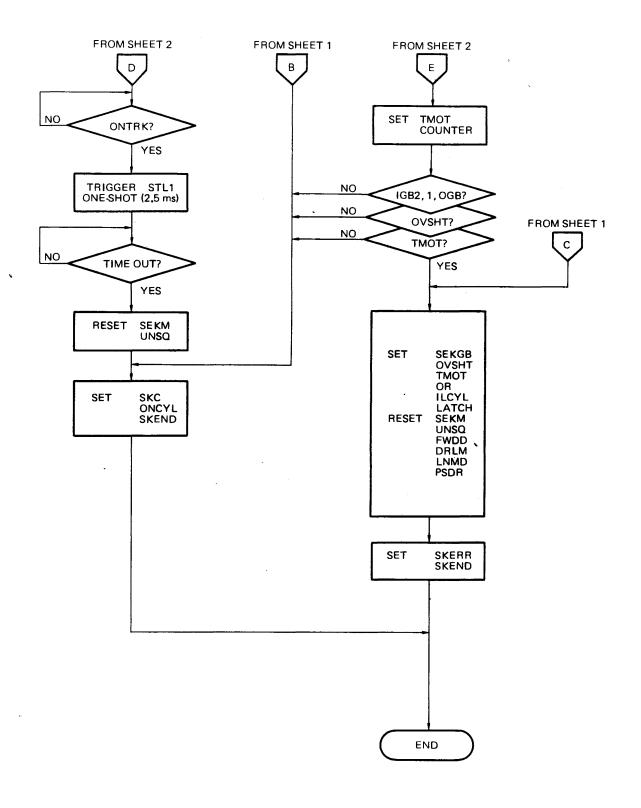
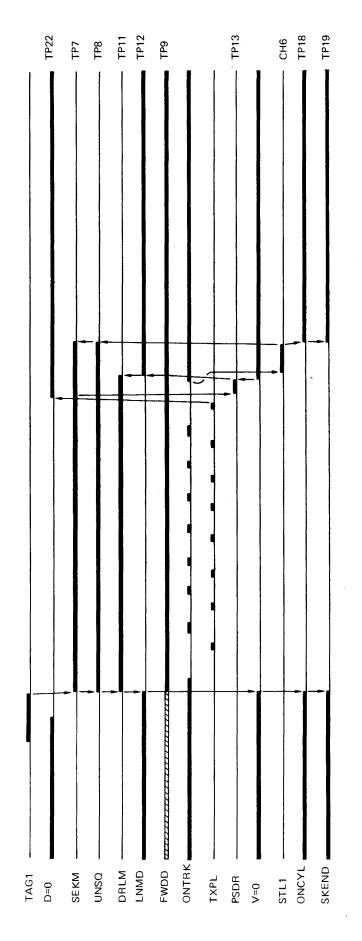


Figure 4-6-13 Direct Seek Flow Chart (Sheet 3 of 3)



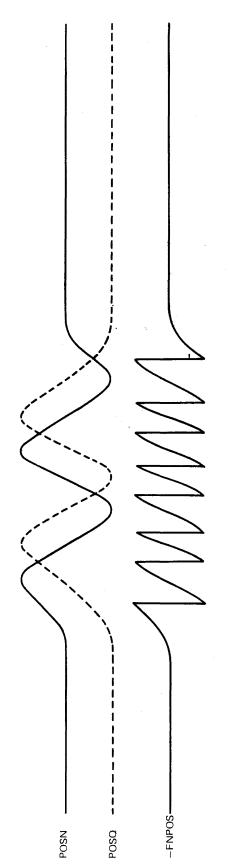


Figure 4-6-14 Direct Seek Timing Chart

4.6.4.4 Servo Off Mode

If a seek malfunction shown in Table 4-6-1 occurrs in the drive, all servo modes (INSKM, GTZM, SEKM, and LNMD) are reset and the heads move to the Landing Zone by the mechanical force of the retract spring in the actuator assembly.

Table 4-6-1 Seek Malfunctions

ERROR	UNIT STATUS
Initial Seek Time Out Rotational Speed High or Low DC voltage fault	Not Ready Not Ready Not Ready
Time Out in Any Seek Mode Over-shoot in Linear Mode Any Guard Band in Seek Mode OGB in Go To Zero Mode	Seek Error Seek Error Seek Error
Any Guard Band in Linear Mode Illegal Cylinder	Seek Error Seek Error Seek Error

4.6.5 Servo Circuit Function

4.6.5.1 Position Sensing

This section describes the Position Sensing functions from the output of the servo head to generating the position signal. The Position Sensing block diagram is shown in Figure 4-6-15.

The servo data written on the servo surface is read by the servo head, amplified through the Head-Preamplifier (with a nominal gain of 35), and applied to the Automatic Gain Control (AGC) amplifier on CMZM PCB. The AGC amplifier keeps the output constant with an AGC voltage from the Summing Amplifier, even if the AGC input varies. The AGC output is applied to a Low Pass Filter (LPF), which attenuates the unused high frequencies, and then is amplified by the Carrier Amplifier. The Carrier Amplifier issues the Servo (SERVO) signal of four-byte interval to the Level Slice and Peak Hold circuits.

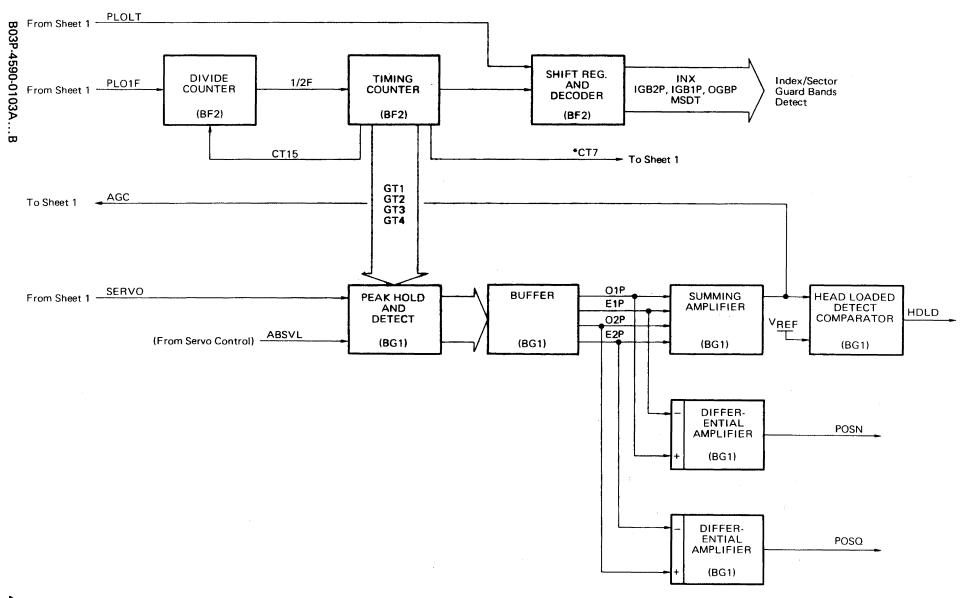


Figure 4-6-15 Position Sensing Block Diagram (Sheet 2 of 2)

The SERVO signal is converted into the Servo Slice Output (SVSLT) signal at a TTL level. The SVSLT signal triggers a 100 ns pulse at its trailing edge and the trailing edge of this 100 ns pulse triggers the 310-ns-long Servo Pulse Window (SVPWD) one-shot. The SVPWD signal separates only the Sync Pulse, that is, it separates the Servo Pulse (SVPLS) signal from the SVSLT signal. The SVPLS Signal is applied to the Phase Locked Oscillator (PLO).

The leading edge of the SVPLS Signal triggers PLOSS one-shot (1.5 μ s) and sets the PLO Latch circuit. The PLO Latch is reset by the leading edge of the Count 7 (CT7) signal, which is the output signal of the Timing Counter, and issues the PLO Latch (PLOLT) signal to the Phase Comparator circuit and the Index Guard Bands sense circuit.

The PLOSS and PLOLT signals are applied to the Phase Comparator circuit of PLO. The Phase Comparator issues and Increase (INC) signal when phase-lag has occurred on the VCO output, or a Decrease (DEC) signal when phase-lag has occurred on the VCO output. The INC and DEC signals are applied to the Charge Pump circuit which converts the phase difference into a DC-levle signal. The Charge Pump circuit issues a control voltage to the Voltage Controlled Oscillator (VCO) through the Low Pass Filter (LPF). Thus, the PLO circuit synchronized with the SVPLS signal and generates a one-bit cell clock, that is, the PLO1F signal. The PLO1F signal is applied to the VFO circuit and the Timing Counter circuit.

The Timing Counter circuit divides the PLO1F signal by two into 1/2F signal. The 1/2F signal generates the Gate 1, 2, 3, and 4 (GT1 to GT4) signals Count 15 (CT15), which reset the divide counter and the CT7 signal, which resets the PLOLT signal.

The Peak Hold circuit holds the position of the peak signals (Odd 1, Even 1, Odd 2 and Even 2) enabling the GT1 to GT4 timing signals. The Peak-hold outputs (Odd 1 peak, Even 1 peak, Odd 2 peak, and Even 2 peak) are applied to the Summing Amplifier and two Differential Amplifier circuits.

The Differential Amplifiers issue the Position Normal (POSN) signal from Odd 1 peak and Even 1 peak signals, and the Position Quadrature (POSQ) signal from Odd 2 peak and Even 2 peak signals. The Summing Amplifier issues the AGC Control Voltage (AGC) signal for the AGC amplifier. When the AGC signal exceeds the reference level, the Head Loaded (HDLD) signal is issued to the seek control circuit. The timing chart for PLO and Peak Hold is shown in Figure 4-6-16. The conversion waveform for Servo signal to dual-phase position signal is shown in Figure 4-6-17, which is valid when the servo head is moving.

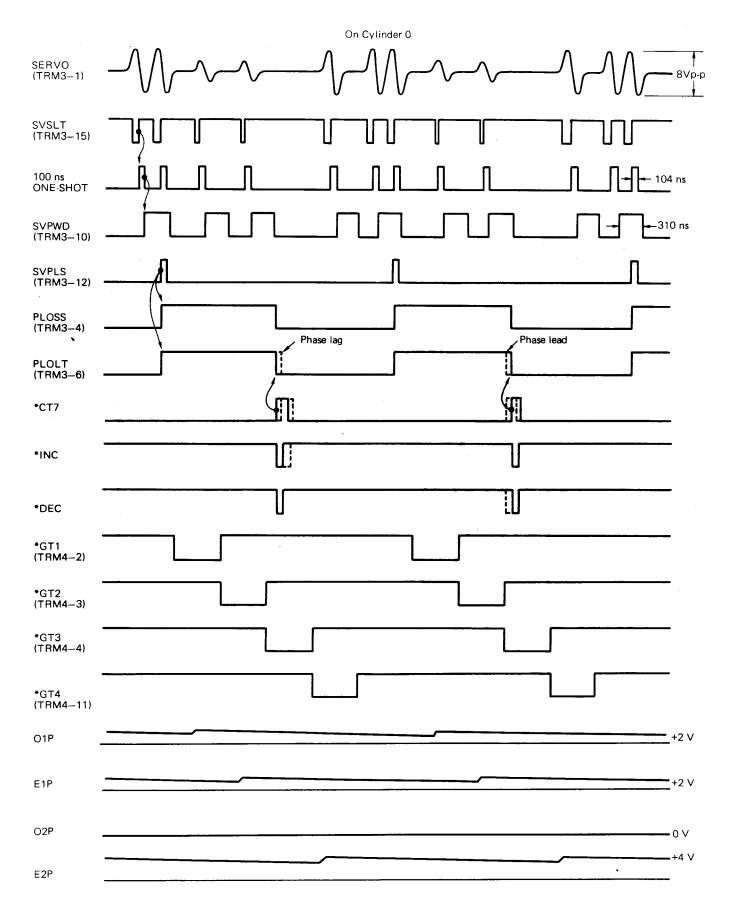
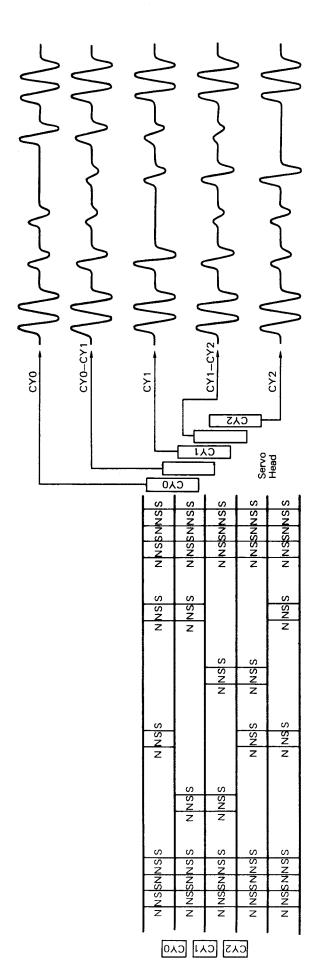


Figure 4-6-16 PLO and Peak Hold Timing Chart



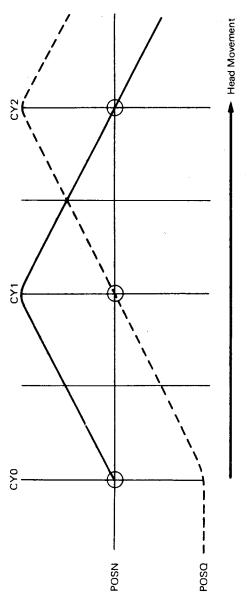


Figure 4-6-17 Servo Signal to Position Signal Conversion

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4.6.5.2 Servo Control

The block diagram of the Servo Control circuit after Position Sensing is shown in Figure 4-6-18.

- (1) Block Description
 - a) Position Signal Slice

The dual-phase position signals, POSNand POSQ, which are demodulated through Position Sensing circuitry, are applied to a level slice circuit. The Position Signal Slice circuit then issues N > Q and N + Q > 0 signals which are applied to Position Decoder, also issues an Off-track (OFTRK) signal which indicates that the servo head positions off from the center of each cylinder by $\pm 2~\mu m$.

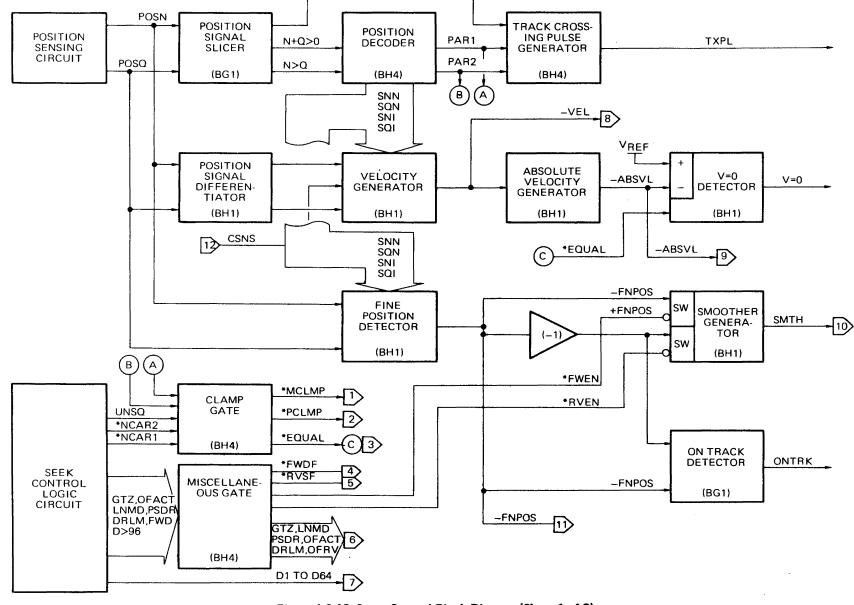


Figure 4-6-18 Servo Control Block Diagram (Sheet 1 of 2)

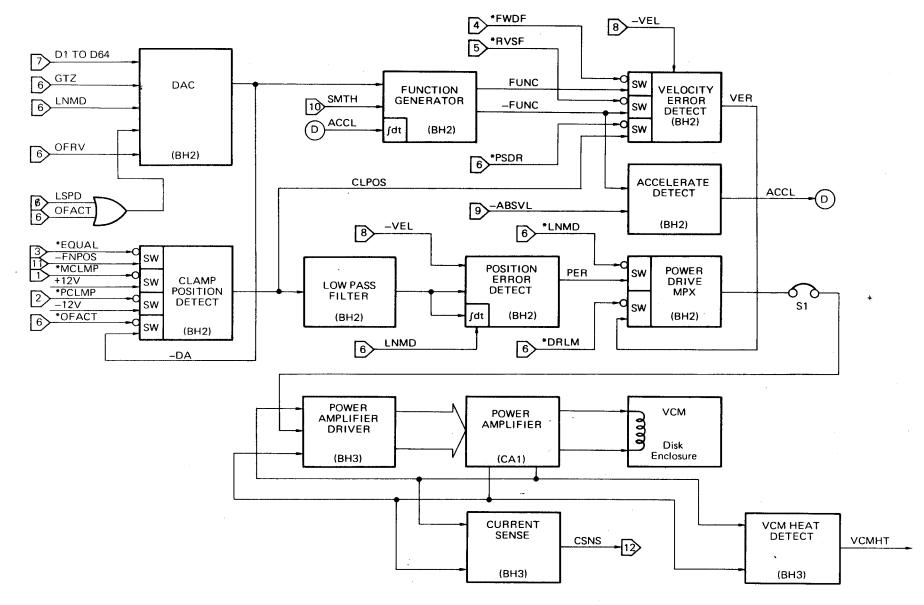


Figure 4-6-18 Servo Control Block Diagram (Sheet 2 of 2)

b) Position Decoder

The Position Decoder circuit issues two least-signaificant bits of the current cylinder address, Present Address 2 and 1 (PAR2 and PAR1), which decode the N > Q and N + Q > 0 signals. The Position Decoder circuit also issues Select N Non-invert (SNN), Select Q Non-invert (SQN), Select N Invert (SNI), and Select Q Invert (SQI) signals, which control the Velocity Generator circuit and Fine Position Detector circuit.

c) Track Crossing Pulse Generator

The Track Crossing Pulse Generator circuit issues a 15- μ s-wide Track Crossing Pulse (TXPLS), which is generated by PAR2, PAR1, and OFTRK signals, and which is applied to the Present Cylinder Address Register (PCAR). The PCAR counts up the TXPLS signal when Forward Drive (FWDD) signal is true, and counts down when FWDD signal is false.

The timing chart for items (1) through (3) is shown in Figure 4-6-19.

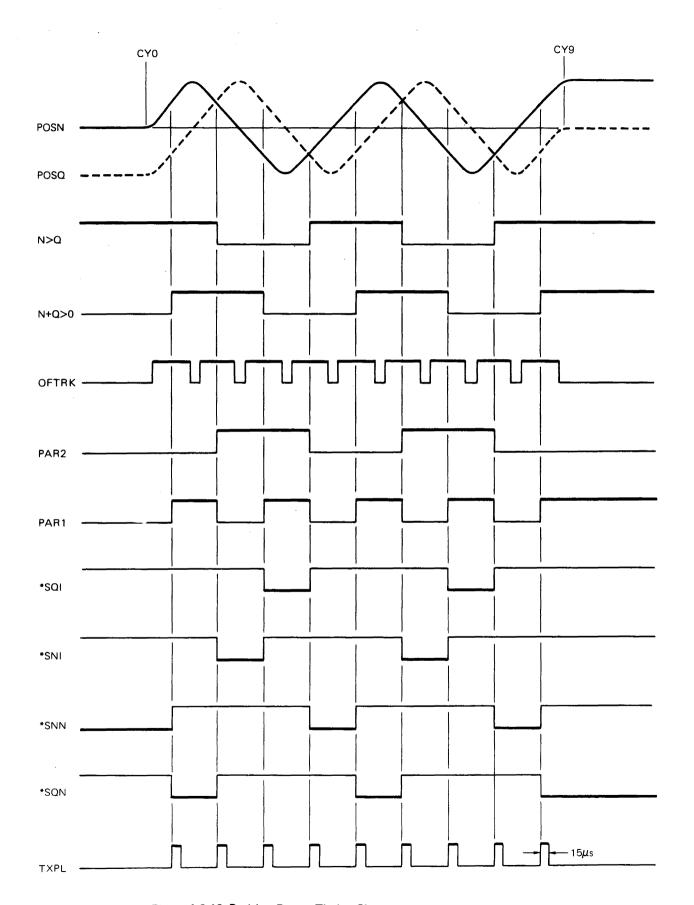


Figure 4-6-19 Position Detect Timing Chart

- d) Position Signal Differentiator
 - The Position Signal Differentiator circuit differentiates the dual-phase position signals, POSN and POSQ, to generate the actual velocity from the linear portion of the position signal.
- e) Velocity Generator
 - The SQI, SNI, SNN, and SQN signals, which are issued from the Position Decoder circuit, pull out the linear protion of the position signals; the composed signal and Current Sense (CSNS) signal are then converted into the Velocity (VEL) signal.
- f) Absolute Velocity Generator
 - The Absolute Velocity Generator converts the velocity signal, with polarity, into the Absolute Velocity (ABSVL) signal.
- g) V = 0 Detector
 - When the Equal signal on the Clamp Gate circuit goes true, and when the velocity is within 1 cm/second, the Velocity Equal to Zero (V = 0) signal is issued to the Seek Control circuit and then the Seek mode is changed to Linear mode by terminating Seek operation.

The timing chart of the Velocity Generator is shown in Figure 4-6-20.

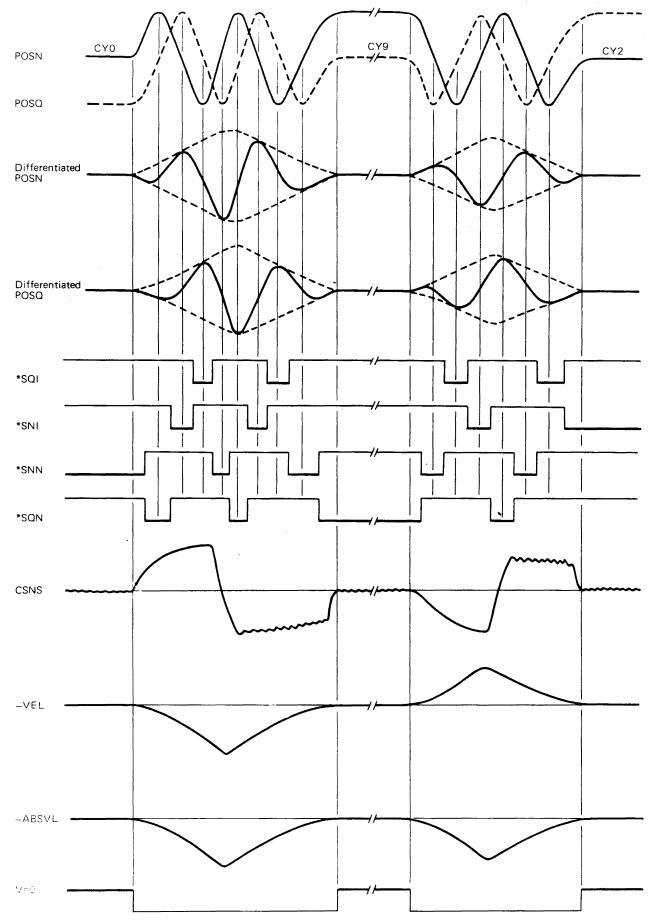


Figure 4-6-20 Velocity Generator Timing Chart

- h) Fine Position Detector
 - The Fine Position Detector circuit pulls out the linear position, that is, the Fine Position (FNPOS) signal the from the POSN and POSQ signals controlled by SQI, SNI, SNN, and SQN signals. The FNPOS signal is applied to the Smoother, On Track Detector, and Clamp Position Detector circuits.
- i) Smoother Generator
 - The Smoother Generator circuit polarizes the FNPOS (the polarity of signal which is in accord with the head movement direction) and issues the Smoother (SMTH) signal. The SMTH signal makes the DA signal smooth through the Function Generator circuit (see item (12), below). When the difference between NCAR and PCAR, however, is greater than 96 during Direct Seek mode, or GTZ mode is activated then the SMTH signal is deactivated.
- i) On Track Detector

The On Track Detector senses the servo head positions on the center of each cylinder within $\pm 4~\mu m$ and issues an On Track (ONTRK) signal to seek control and fault detect logics.

The timing chart of Fine Position Detect is shown in Figure 4-6-21.

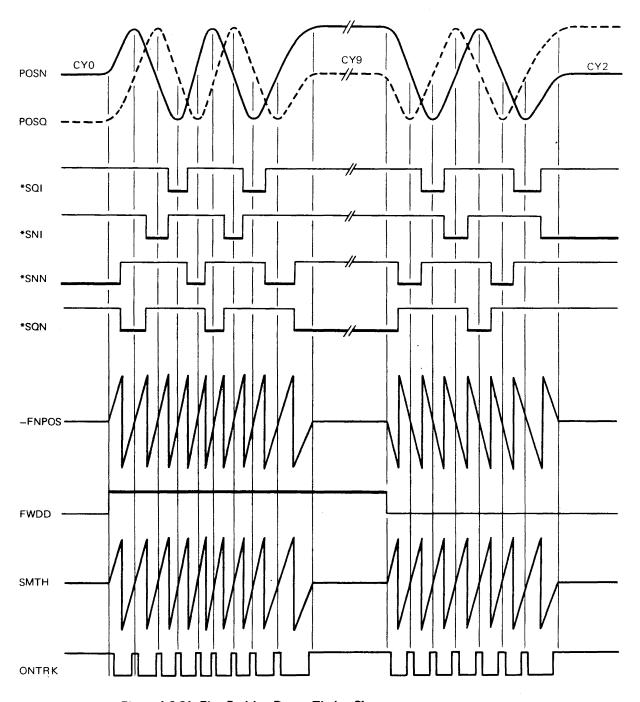


Figure 4-6-21 Fine Position Detect Timing Chart

k) DA Converter

The DA Converter DAC circuit generates the target velocity during Direct Seek or GTZ operations. When the Direct Seek operation is performed, the Difference Counter bits D1 to D64 are applied to the DAC at the beginning of the seek operation. Whenever the servo head has passed through each cylinder, the TXPLS signal is issued and it decreases the Difference Counter. When the Difference Counter output is equal to or greater than 96, the D1 to D64 signal is clamped to 96 and the DAC output is adjusted to be -6.8 V.

When the GTZ operation is performed, GTZ and LSPD signals set a target velocity through the DAC.

When the Offset operation is performed, OFACT and OFRVS signals set the offset voltage to a value equivalent to $\pm 3~\mu m$ from the center of cylinder. The DAC output, -DA signal, is applied to the Function Generator and Clamp Position circuits.

I) Function Generator

When the Difference Counter output is less than 96, the Function Generator circuit converts the DAC output into a smooth waveform by adding the SMTH signal. The Function Generator issues a Function (FUNC) signal which is the optimum deceleration curve for position time and the deceleration current profile.

When the servo control is changed to deceleration from acceleration, the Function Generator adds the integrated ACCL signal to the FUNC signal to avoid an excessive force to the actuator.

m) Velocity Error Detector

The Velocity Error Detector circuit issues the Velocity Error (VER) signal, which is applied to the Power Amplifier, after comparing a target velocity (FUNC) signal and actual velocity (VEL) signal. At the termination of Seek operation, the Clamped Position (CLPOS) signal is applied to the Velocity Error Detector instead of the FUNC signal, which activates the PSDR signal.

n) Accelerate Detector

The Accelerate Detector output, that is, the Accelerate (ACCL) signal, is set by the leading edge of the DRLM signal and reset when the ABSVL signal is equal to the FUNC signal. The ACCL signal is applied to the Function Generator circuit.

The timing chart of the Target Velocity Generator, for a Direct Seek operation, is shown in Figure 4-6-22, and the timing chart for a GTZ operation is shown in Figure 4-6-23.

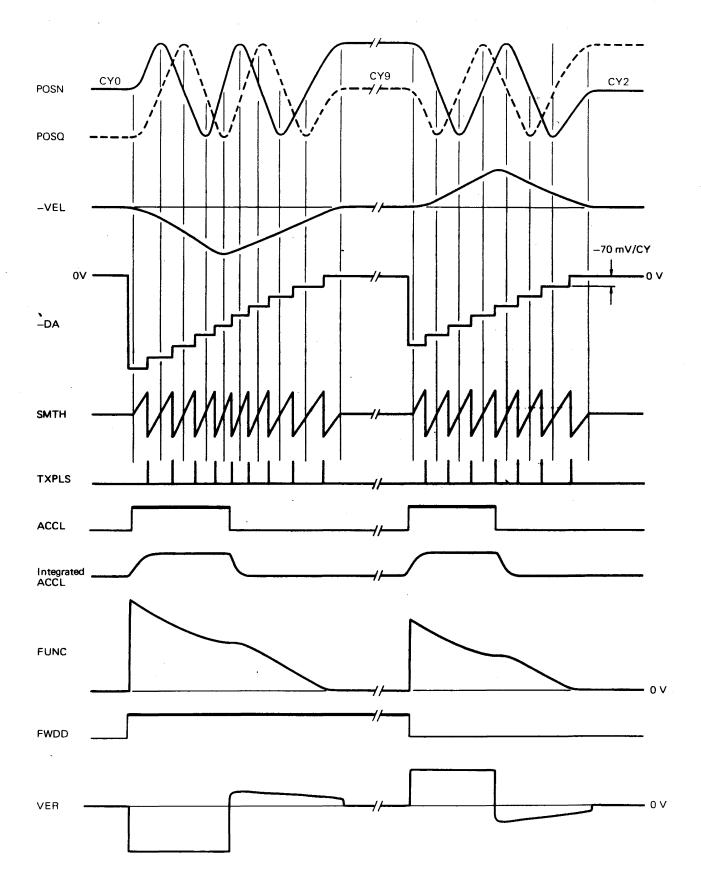


Figure 4-6-22 Direct Seek Target Velocity Generator

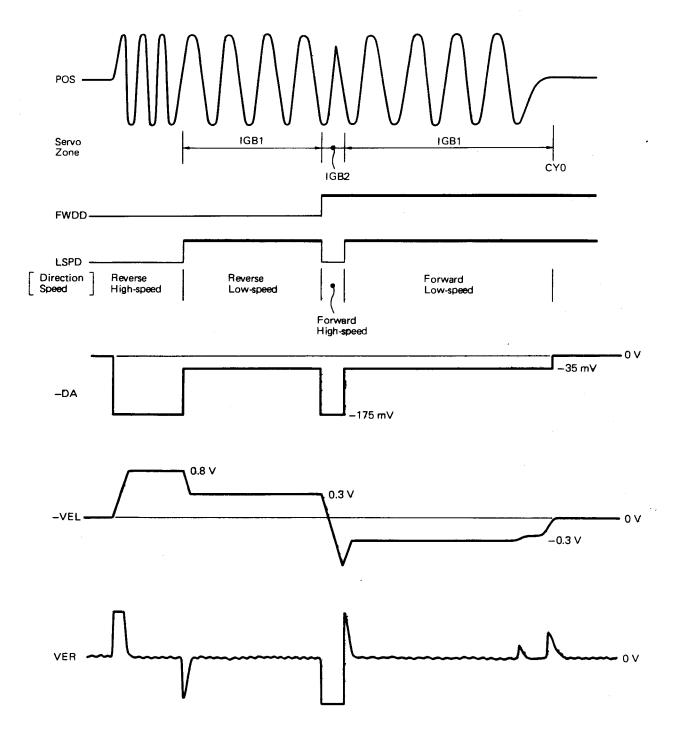


Figure 4-6-23 GTZ Target Velocity Generator

p) Clamp Gate

The Clamp Gate circuit issues Minus Clamp Position (MCLMP), Plus Clamp Position (PCLMP) and Equal (EQUAL) signals through the adder circuit, which compares the two least-significant bits (NCAR2 and 1) of the target cylinder (NCAR2 and NCAR1) with PAR2 and PAR1 signals from the Position Decoder circuit.

q) Clamp Position Detector

The Clamp Position Detector holds the position signal at specified levels when the servo head is positioned within three cylinders of the target cylinder address specified by the two least-significant bits of NCAR and PAR. This extends the area controlled by the servo circuit.

The PCLMP signal sets the Calmped Position Signal (CLPOS) to +2 V, the MCLMP is set to -2 V, and the EQUAL signal enables the FNPOS signal on the CLPOS signal.

The CLPOS signal is applied to the Velocity Error Detector circuit when the PSDR signal goes true at the termination of Seek operation, and is then applied to Low Pass Filter (LPF) when the servo head settles on the specified cylinder.

The timing chart of Clamp Position is shown in Figure 4-6-24.

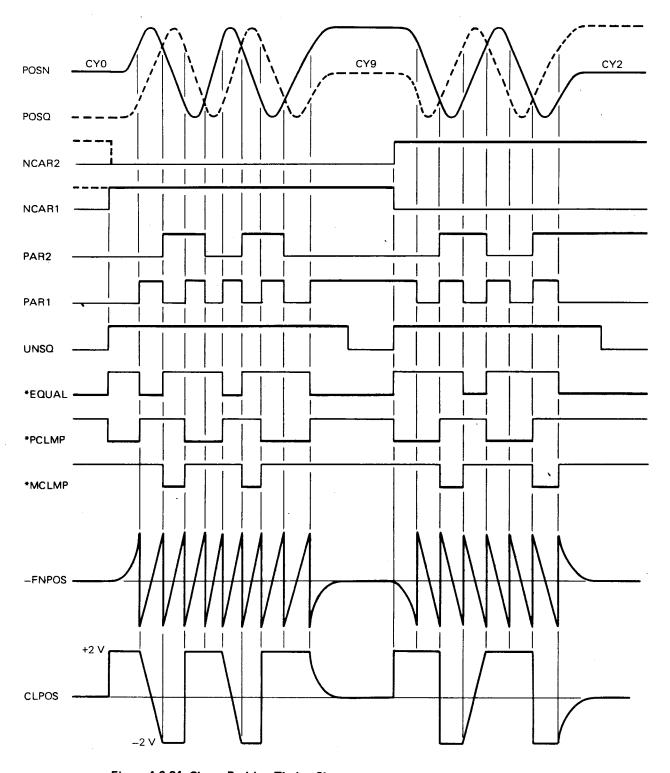


Figure 4-6-24 Clamp Position Timing Chart

r) Low Pass Filter (LPF)

The servo circuits form a feed-back loop during track following after a Seek operation using the position signal recovered from the servo head.

The LPF circuit attenuates unused high frequencies. The LPF has a resonance frequency at 1.9 KHz.

s) Position Error Detector

The Position Error Detector pulls out the phse-compensated Position Error (PER) signal required for the feed-back loop during track following.

The PER signal is composed of a VEL (phase-compensating) signal, and an integrated position signal; improves stiffness and following characteristics of lower frequencies.

t) Power Drive Multiplexer

The Power Drive Multiplexer circuit passes through either the VER signal, by activating DRLM signal during Direct seek or GTZ operation, or the PER signal, by activating the LNMD signal during track following sequence.

u) Power Amplifier Driver

The Power Amplifier Driver circuit drives the last stage of the power amplifier. This circuit controls the base current to the power transistors by comparing the input signal with the feed-back signal from the last-stage transistor current.

v) Power Amplifier

The Power Amplifier circuit is a current amplifier which drives the coil of the Voice Coil Motor (VCM). The circuit is composed of four H-type transistors.

w) Current Sense

The Current Sense circuit detects the VCM coil current through the voltage bleeder resistors. The coil current is amplified by the differential mode, and then the Current Sense (CSNS) signal is issued.

x) VCM Heat Detect

The VCM Heat Detect circuit senses an abnormal current flowing through the VCM coil or also DC Motor windings.

The coil current of the DC Motor windings current is integrated and converted into the VCM Heat Detect (VCMHT) signal.

(2) Direct Seek Servo Control

During a Direct Seek with servo control, the servo head is driven high speed, so that the actual velocity pulled out from the position signal through the servo head is equal to the target velocity controlled by the Difference Counter. Whenever the servo head has passed through each cylinder, the target velocity is decreased for optimum speed control. The Direct Seek signal flow is shown in Figure 4-6-25.

(3) GTZ Servo Control

Wherever the head is positioned, GTZ Servo Control returns the head to Cylinder 0. The target velocity is given by the specified velocity, that is, high speed is 8 cm/second and low speed is 3 cm/second.

The GTZ signal flow is shown in Figure 4-6-26.

(4) Linear Mode Servo Control

When the servo head is positioned within capture distance from the spcified cylinder, the Servo Control mode is changed to Linear mode. During Linear mode (track following), the feed-back loop is formed to minimize the Position Error Signal.

When an Offset operation is performed, the offset voltage is applied to the Position Error signal through the DAC. The servo head is the offset by $\pm 3~\mu m$.

The Linear mode signal flow is shown in Figure 4-6-27.

OFTRK

Figure 4-6-25 Direct Seek Signal Flow (Sheet 1 of 2)

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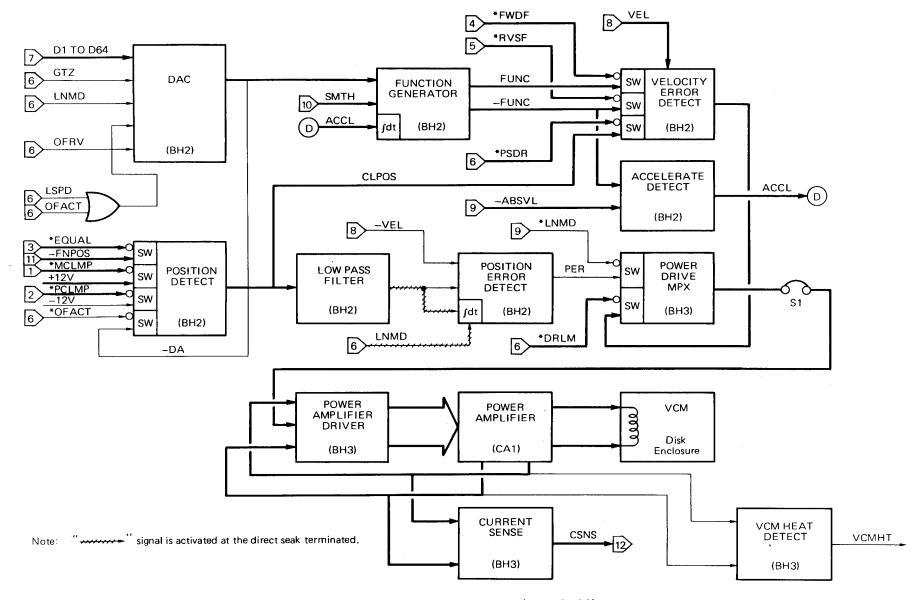


Figure 4-6-25 Direct Seek Signal Flow (Sheet 2 of 2)

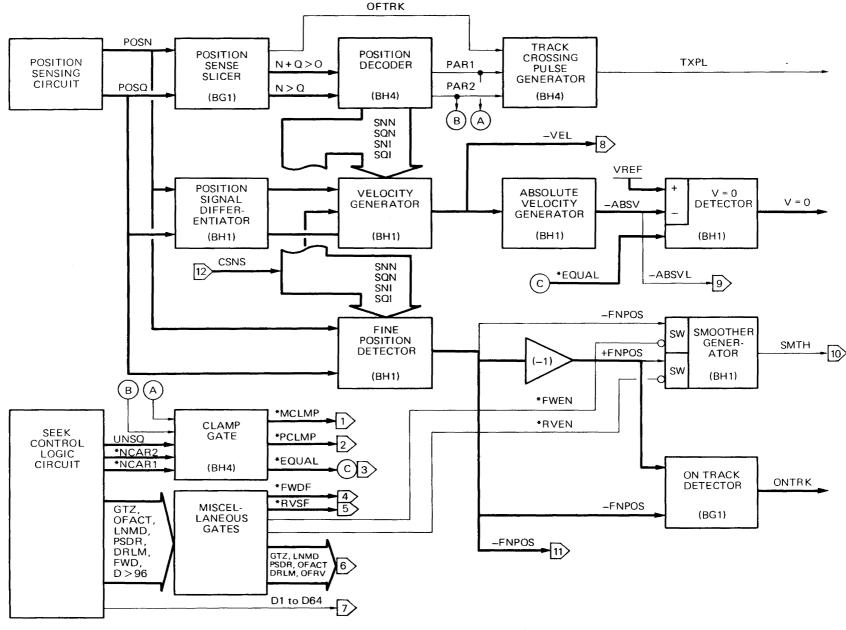


Figure 4-6-26 GTZ Signal Flow (Sheet 1 of 2)

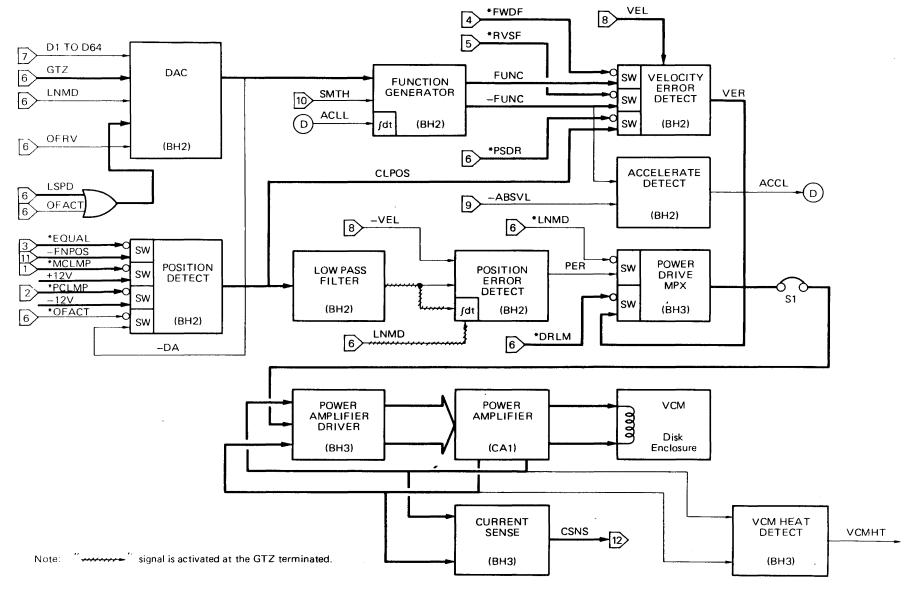


Figure 4-6-26 GTZ Signal Flow (Sheet 2 of 2)

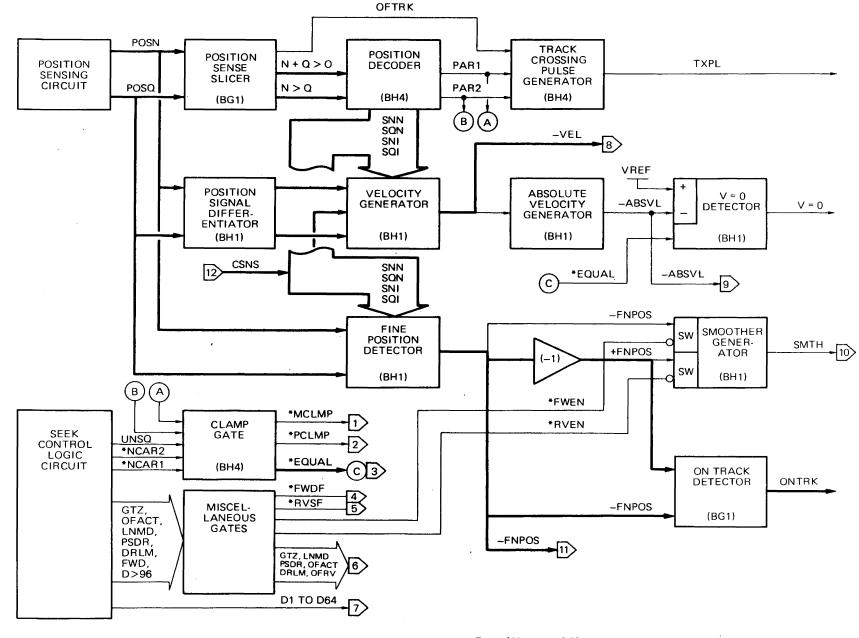


Figure 4-6-27 Linear Mode Signal Flow (Sheet 1 of 2)

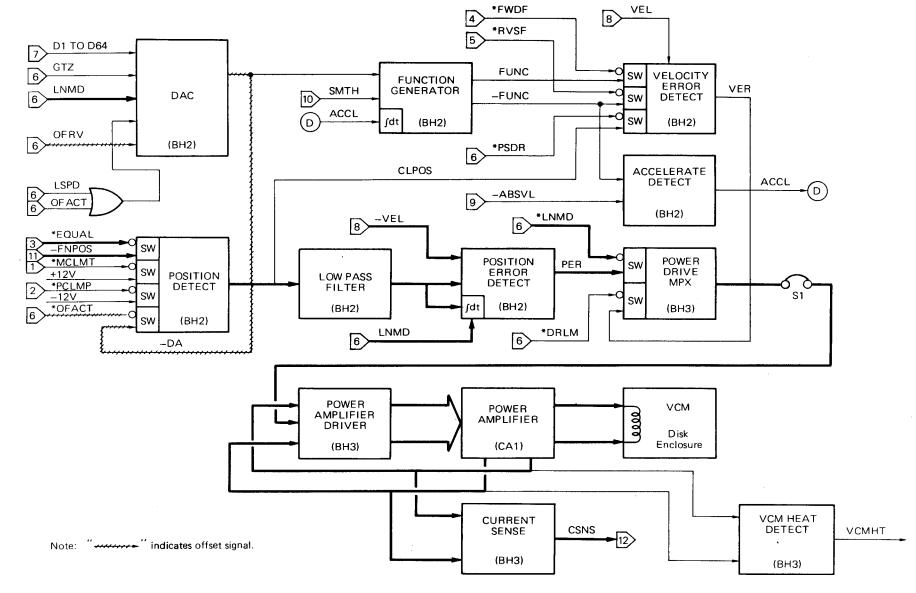


Figure 4-6-27 Linear Mode Signal Flow (Sheet 2 of 2)

4.6.6 Index/Sector/Guard Band Generate Function

4.6.6.1 Index Detect

As described in the position sensing discussion, the servo signal contains missing Index Bits. The servo pulse (SVPL) is applied to the PLO which outputs a one-bit cell closk (PLO1F).

The PLO latch (PLOL) signal is set by the leading edge of the SVPL signal and reset by the leading edge of Count 7 (CT7). It is applied to a shift register and clocked by the positive-going edge of the CT7 signal.

The shift register outputs are decoded, and then the Index (INX) signal, two Inner Guard Band pulse (IGB2P and IGB1P) signals, and the Outer Guard Band pulse (OGBP) signals are detected by the combination of the decoder outputs. The block diagram of Index and Guard Band pattern detect is shown in Figure 4-6-28. The timing chart of the Index signal processing is shown in Figure 4-6-29.

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Figure 4-6-28 Index/Guard Band Patterns Detect Block Diagram

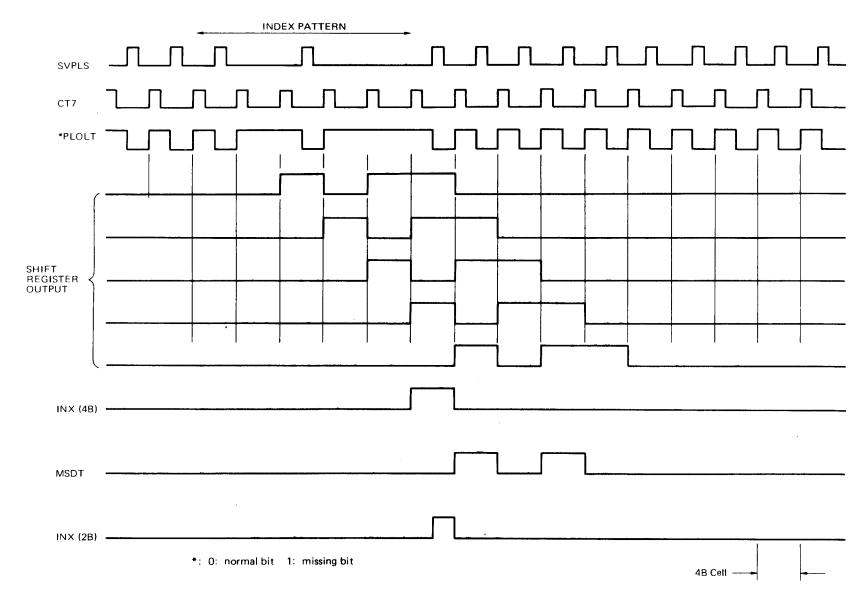


Figure 4-6-29 Index Detect Timing Chart

4.6.6.2 Guard Band Detect

As described in Section 4.3.3, each guard band has a missing Index bit. When the servo head is located on any guard band track, the servo PLO circuit develops IGB2P, IGB1P, or OGBP and missing detect (MSDT) signals as shown in Figure 4-6-30.

The first pulse of the Guard Band Pulse sets the first flip-flop, and simultaneously the MSDT signal loads 187 (decimal) on the Guard Band Reset counter clocked by the four-byte interval Count 15 (CT15) signal. The second pulse sets the second flip-flop; Guard Band signal (IGB2, IGB1, or OGB) is then issued to the seek control logic. This occurs it the second pulse goes true before the Guard Band Reset Counter issues the Reset Guard Band (RSTGB) signal at 255 (decimal) (within a 276-byte interval).

The output of each Guard Band latch output is reset by a RSTGB signal. When the servo head is not located over a guard band track, or when the servo head has passed through Guard Band (IGB2) to Guard Band 2 (IGB1) in the reverse direction.

Two continuous pulses of imcompatible Guard Band signals are detected when the servo head passes from Guard Band 2 into Guard Band 1.

The two stages of the flip-flop prevent the Guard Band signal from improper detection of the Guard Band Pulse signals caused by media flaws.

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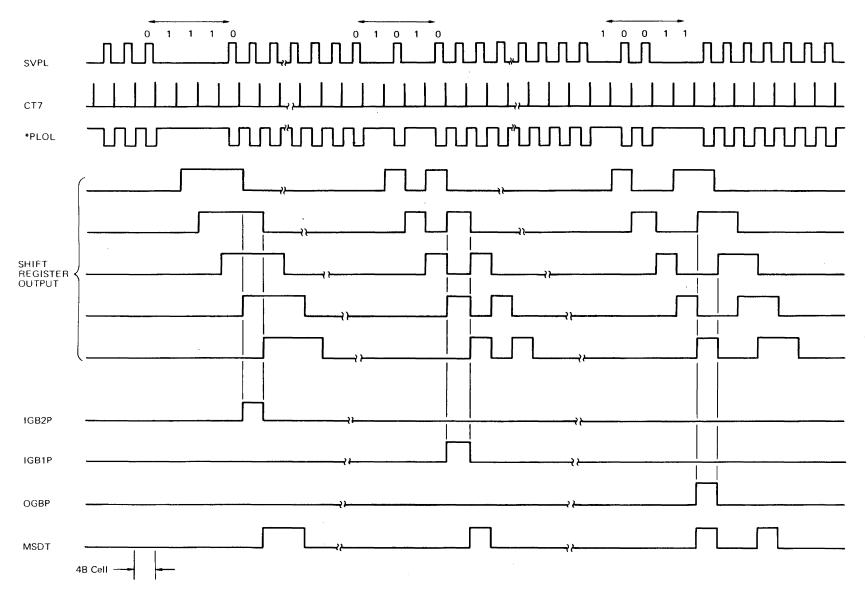


Figure 4-6-30 Guard Band Pulse Detect Timing Chart

4.6.6.3 Sector Generator

A Sector pulse is not written on the servo surface. The sector pulses are derived from a Byte counter counting Byte clocks, which are generated by the PLO circuit synchronized with servo pulse. One disk revolution has 20,480 Byte clocks, and the sector length is determined by selectable keys on the CNAM PCB.

The Index signal (Two Bytes) from the PLO circuit enables the preset input to the Byte Counter. The value loaded into the Byte Counter is a 256-byte sector length is specified by turning on SW2 keys one to seven and SW3 key two. The binary value of the keys not turned on (SW3 keys two to seven) equals 65,280. The Index signal causes the Byte counter to be preset to 65,280. The Counter is then clocked by the positive going edge of the Byte Clock (BYTCL) signal until it reaches 65,535 (255 byte clocks). The next BYTCL signal would then cause a carry signal which is used as a new preset enable to the Byte Counter. The carry signal is applied to next flip-flop and then converted into 12-bit pulse of the Sector signal. The block diagram is shown in Figure 4-6-28, and the timing chart is shown in Figure 4-6-32:

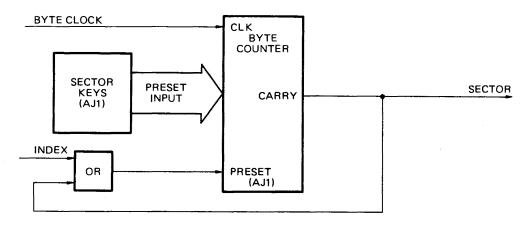


Figure 4-6-31 Sector Generator Block Diagram

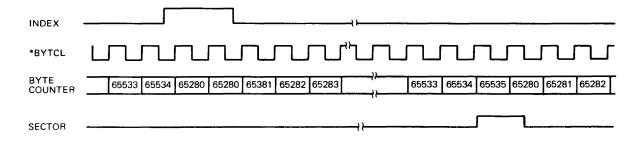


Figure 4-6-32 Sector Generator Timing Chart

4.6.7 Head Selection

A head must be selected before a read or write operation can be performed. The head address is set by the positive-going edge of the Tag 2 signal with Bus bit 0 to 2 at the Head Address Register (HAR). The HAR outputs, HAR1, 2 and 4 signals, are applied to the CNAM PCB. The signal (HAR4) is decoded into chip select 0 and 1 (CS0 and CS1: ECL level) and then applied to head ICs in the disk enclosure. Lower bits HAR1 and 2 are converted into head select 1 and 2 (HS1 and HS2: ECL level).

The DC regulators supply +6 V DC (Vcc) and -4 V DC (Vee) to the head ICs within the disk enclosure. The multiple-chip select or head-short condition is detected by an overload current of Vcc supply. The block diagram of head selection is shown in Figure 4-6-33.

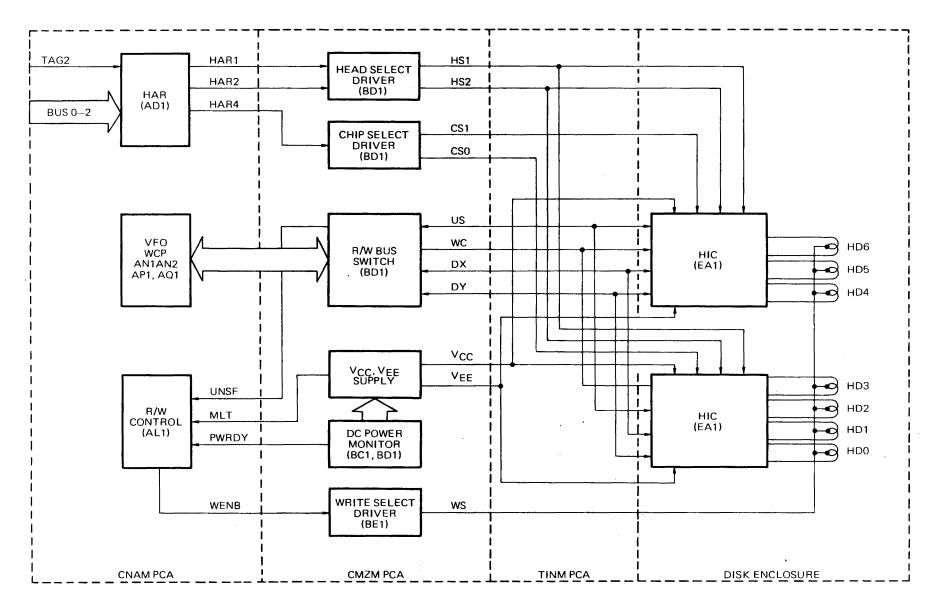


Figure 4-6-33 Head Selection Block Diagram

4.6.8 Read/Write Function

4.6.8.1 Read/Write Basic Principles

When the disk is rotating at a nominal 3,600 rpm, a read or write may be performed. The basic principles of the read/write function are as follows:

(1) Data Write

During a write instruction, a 0 or 1 is recorded by reversing the direction of the current flowing in the data head coil. When the direction of the current flowing in the head coil is reversed, the magnetic poles of the head are reversed and the direction of magnetic flux at the gap is reversed. The direction of magnetization of the surface of the disk is then reversed. Each flux reversal means that a "1" or "0" has been recorded on the disk.

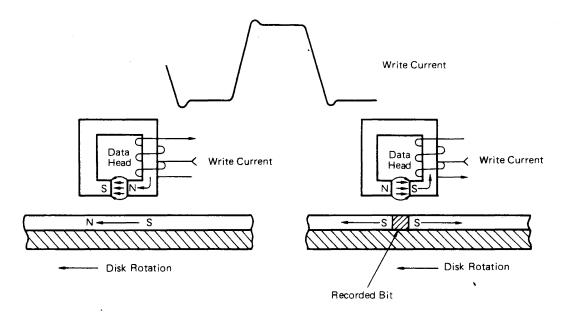


Figure 4-6-34 Data Write

(2) Data Read

During a read instruction, the transitions recorded on the surface of the disk are detected by the head gap. When magnetized in the same direction continuously, no output is produced. However, when a recorded bit (180-degree flux reversal in the horizontal direction) passes under the head gap, the magnetic flux flowing in the ring and coil is reversed and an output pulse is obtained.

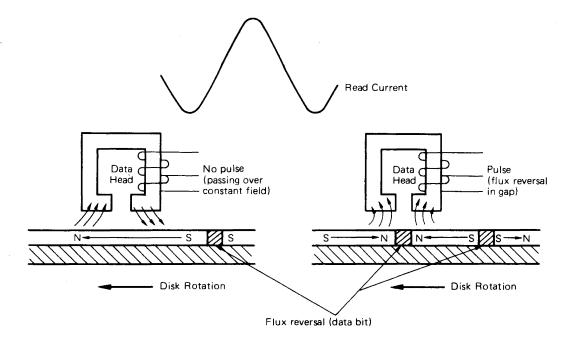


Figure 4-6-35 Data Read

(3) Principles of MFM Recording

This unit uses the modified frequency modulation (MFM) recording technique. The length of time required to define one bit of information is the cell. Each cell is nominally 102 ns in width.

MFM defines a "1" by writing a pulse at the half-cell time. A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is clock (1 FW). However, clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell. See Figure 4-6-36.

The rule for MFM recording is summarized:

- (A) There is a flux transition for each "1" bit at the time of the "1".
- (B) There is a flux transition between each pair of "0" bits.
- (C) There is no flux transition between the bits of a "10" or "01" combination.

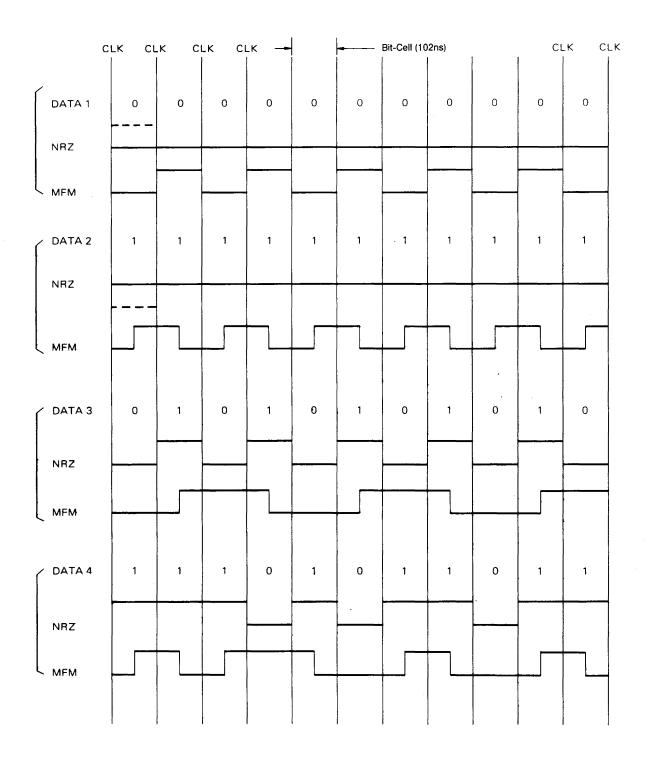


Figure 4-6-36 MFM Coding

4.6.8.2 Write Operation

The write circuit block diagram is shown in Figure 4-6-37. The servo data written on the disk are read by the servo head, and the PLO circuit generates one bit cell PLO1F signal. The PLO1F signal is applied to the VFO (variable frequency oscillator).

The VFO is synchronized with the PLO1F signal and generates a frequency twice the PLO1F frequency; it then generates VFO1F and VFO2F signal. VFO1F and VFO2F signals are applied to the Write Compensation circuit; VFO1F is also sent to the control unit as the 1F Write Clock signal. The control unit must use this 1F Write Clock signal during Write Clock (WCLK) and Write Data (WDAT) generating.

When a write command is issued from the control unit after head selection, the WDAT and WCLK signals are sent the disk drive, and the WDAT signal is clocked by the positive-going edge of WCLK signal.

The clocked WDAT signal is applied to Write Compensation (WCP) circuit, and then is compensated according to the theory of write compensation. Through the Write Compensation circuit, WDAT of NRZ code is converted into Write Data Pulse (WDP) of MFM code.

When the Write Gate signal goes true, the WDP signal is toggled by a flip-flop and passes through the Read/Write Bus Switch IC. It is then applied to the Head IC (HIC) chips as Data X (DX) and Data Y (DY) signals. The write current is supplied to the selected HIC chip through a Write Current (WC) line.

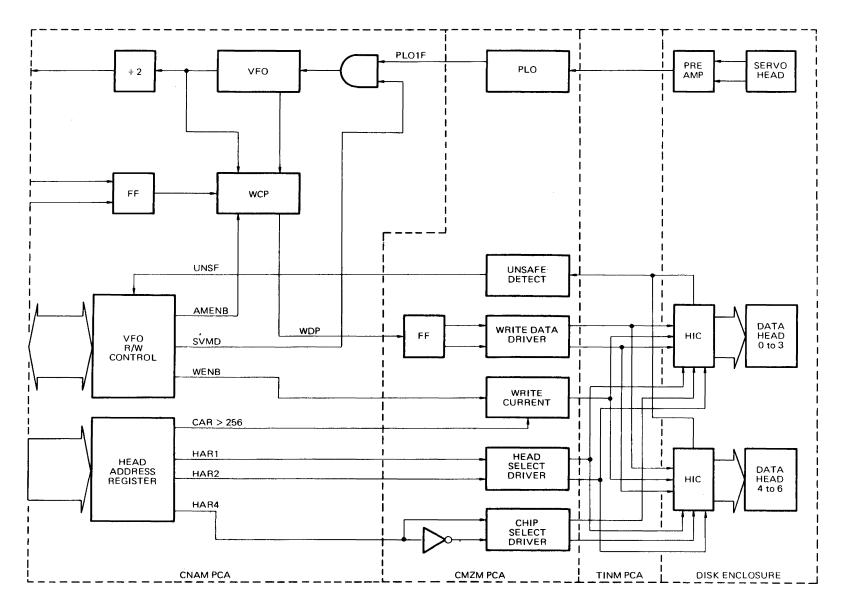


Figure 4-6-37 Write Operation Block Diagram

4.6.8.3 Write Compensation and MFM Coding

When the bit density (BPI) is high on a disk surface, and a read operation is performed, a peak shift phenomenon appears, which tends to widen the narrow part of the bit spacing because of mutual magnetic interference of the bits. When such a phenomenon appears, reading of the data will deviate from the correct bit spacing, causing errors. The write compensation circuit measures this peak shift beforehand so the data is written by shifting the peak in the opposte direction of the peak shift appearing during the read operation.

The NRZ write data (WDAT) sent from the control unit is clocked by the positive-going edge of the WCLK signal. It is then synchronized with the internal one-bit cell clock which issues a sync decision window circuit at the positive-going edge of the Write Enable (WENB) signal.

The NRZ data synchronized with the internal clock is applied to four-bit shift register. Each output of the four-bit shift register is applied to a write compensation decoder and a multiplexer and then converted into a MFM data pulse train with write compensation according to the truth table (as shown in Table 4-6-2). The preshift timing of write compensation is defined by 2F Early (2FEY), 2F On-Time (2FOT) and 2F Late (2FLT) signals.

The block diagram and timing chart are given in Figure 4-6-38 and Figure 4-6-39.

Table 4-6-2 Write Compensation and MFM Truth Table

SHIFT REGISTER STATUS				WRITE COMP			MFM	
SR 0	SR 1	SR 2	SR 3	EYP	ОТР	LTP	CLP	DTP
1	0	0	*	1	0	0	1	0
0	0	0	0	0	1	0	1	0
0	0	0	1	0	0	1	1	0
0	1	*	*	1	0	0	0	1
1	1	1	*	0	1	0	0	1
1	1	0	*	0	0	1	0	1

Note: EYP: Early Pulse

OTP: On-Time Pulse

LTP: Late Pulse CLP: Clock Pulse DTP: Data Pulse

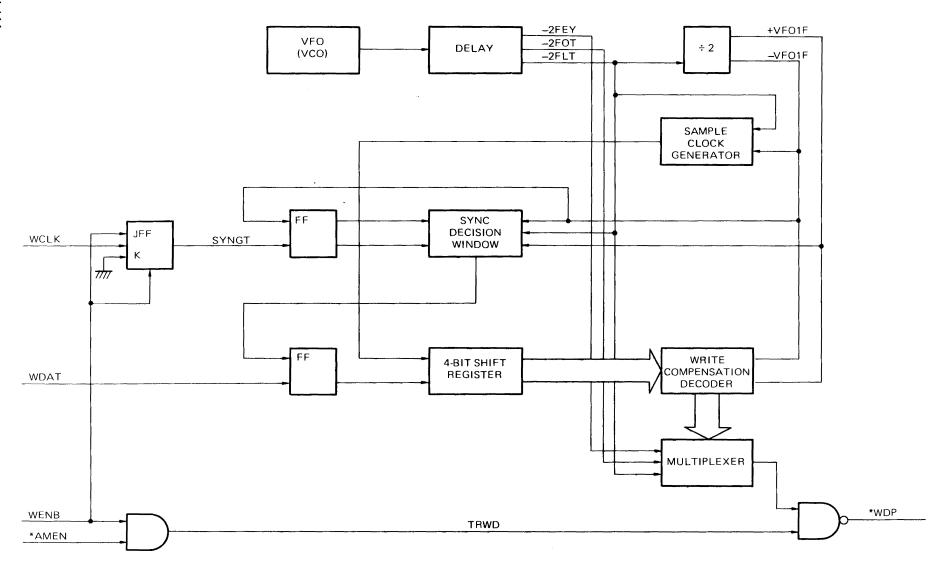


Figure 4-6-38 Write Compensation and MFM Coding Block Diagram

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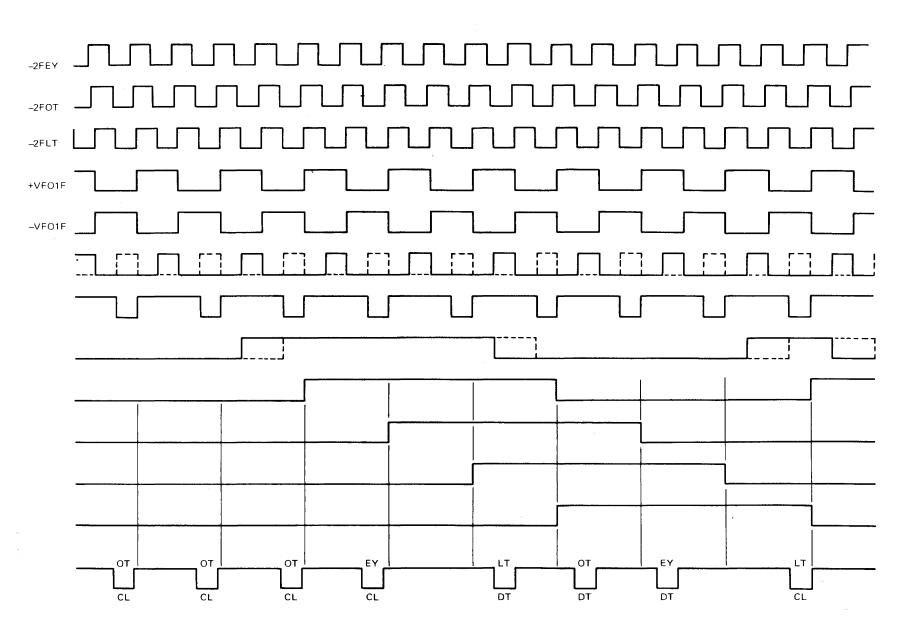


Figure 4-6-39 Write Compensation and MFM Coding Timing Chart

4.6.8.4 Read Operation

A read operation is initiated by enabling Tag 3 and Bus 1 (Read Gate: RG). The analog read circuitry is enabled by disabling Write Enable (WENB).

The DX, DY HIC (Head IC) outputs are applied to the Read/Write Bus Switch IC (MB4316), amplified, and then sent to LPF (Low Pass Filter) circuit as shown in Figure 4-6-40.

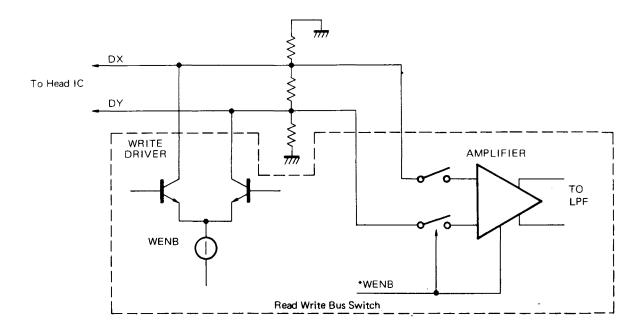


Figure 4-6-40 Read Write Bus Switch

The LPF attenuates the high-frequency noise; its output is then applied to the Automatic Gain Control (AGC) circuit.

The AGC circuit develops the control voltage to the AGC amplifier and holds AGC output amplitude (300 mVp-p) at a constant level. The output of the AGC amplifier is amplified to 3.0 Vp-p, and sent to the Pulse Shaper circuit.

After going false at WENB, the read circuit is activated; however, a read-transient which is caused by the DC unbalance of the read pre-amplifier will occur. WENB signal squelches this read transient (refer to Figure 4-6-41).



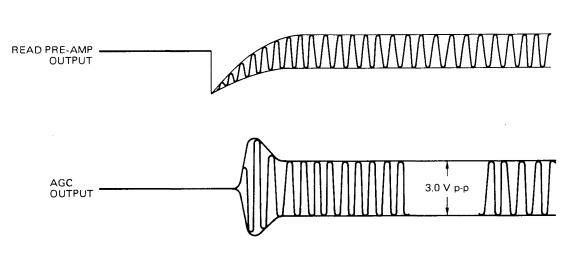


Figure 4-6-41 AGC Squelch Function

In the variable Soft Sector mode, the Address Mark (AM)-which is a DC-erased three-Byte area is used for indicating the beginning of sector. When the control unit issues an AM-Read (Tag 3·Bus 1·Bus 5) command, the AM-Search (AMSH) signal goes true and suppresses the AGC output amplitude to avoid misdetection of an AM caused by external or media noise in the DC-erased area (refer to Figure 4-6-42).

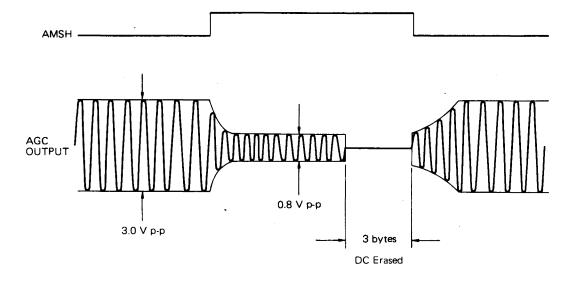


Figure 4-6-42 AM Search on Read Signal

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The analog-to-digital convertor circuit or Pulse Shaper has two fundamental circuits: a differentiator circuit (which differentiates the AGC output signal and then converts the peaks (flux transitions) into zero-crossing signals) and an integrator circuit (which AC-slices the AGC output signal (floating slice) and then generates the data window for the MFM read data pulse). The block diagram is shown in Figure 4-6-43 and the detail timing chart is shown in Figure 4-6-44.

The output of the analog to digital convertor which is raw read data, is sent to the VFO circuit.

4-118

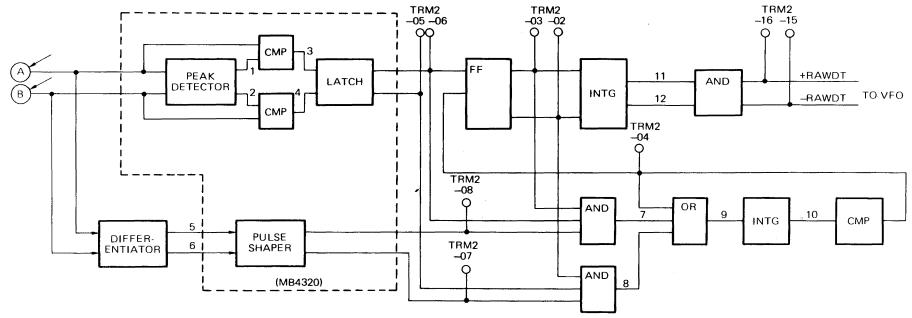


Figure 4-6-43 Read Operation Block Diagram

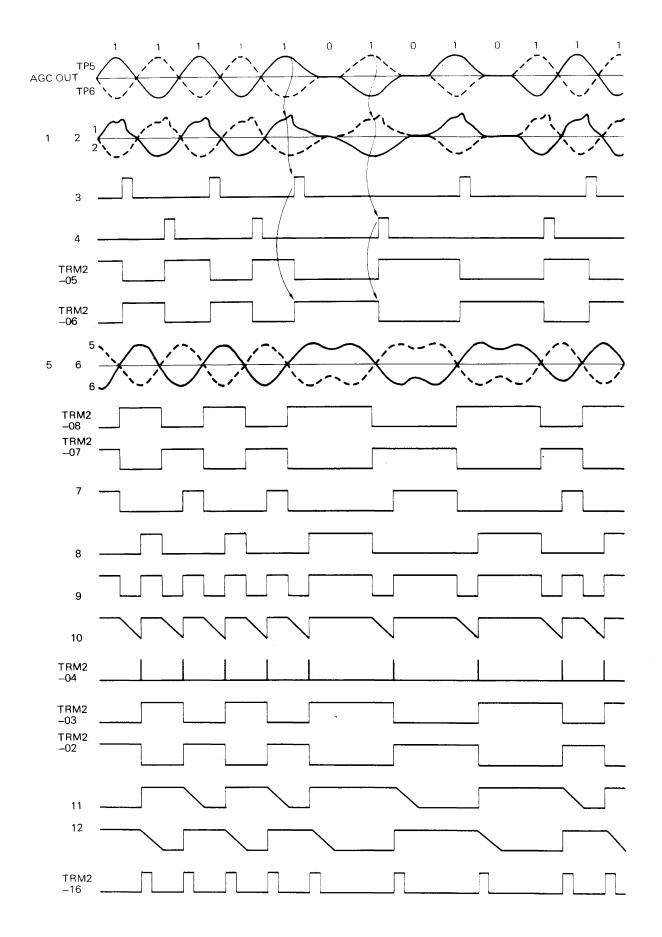


Figure 4-6-44 Read Data Analog to Digital Timing

4.6.9 VFO

4.6.9.1 VFO and Data Separator

The Variable Frequency Oscillator (VFO) circuit synchronizes with a PLO1F signal from the servo track during Not-Read operation and with the Raw Data (RAWDT) signal, from the data track, during a read operation. The block diagram of the VFO and Data Separator circuits is shown in Figure 4-6-45.

The VFO and Data Separator are composed of the following circuit.

- (1) VFO Input Multiplexer
- (2) Time-Margin Measurement (TMG) One-Short
- (3) Reference One-Shot
- (4) Phase-compare Latch
- (5) Phase Comparator and Charge Pump
- (6) Low-Pass Filter and Buffer
- (7) Voltage-Controlled Oscillator (VCO)
- (8) Data Separator

PLO1F

TRM10

–10 Q

TRM10

-11 0

DTIN2

TRM10

-09 Q

CH2

0

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(1) VFO Input Multiplexer

The VFO input multiplexer controls the VFO input. During an initial seek operation or a RTZ operation, this circuit inhibits an input of Data into the VFO circuit by enabling the filter squelch (FLTSQ) signal. This causes the VCO to oscillate at a free-running frequency. After an initial seek operation or RTZ operation, the VFO Input multiplexer controls the transmission of the PLO1F or RAWDT signals into the VFO circuit.

During a Not-Read operation, the PLO1F signal is applied to the VFO circuits by the enabling of the servo mode (SVMD) signal. During a Read operation, the RAWDT signal is applied to the VFO circuits by disabling the SVMD signal. The VFO input multiplexer output, Data In 1 (DTIN1), is applied to the TMG One-shot circuit.

(2) TMG One-shot

The TMG One-shot circuit issues a Data Input 2 (DTIN2) signal to the Phase Comparator, and Reference One Shot. It also issues Delayed Data (DLDT) signal to the Data Separator. The timing relation between DTIN2 and DLDT signals is adjusted by potentiometer RV2 determines the read margin within the VFO circuit.

(3) Reference One-shot

The leading edge of the DTIN2 signal triggers the Reference One-shot, which issues a 19 ns Reference Pulse (REFP) signal to the Phase Comparator Charge Pump circuit.

(4) Phase-compare Latch

The leading edge of the DTIN2 signal sets the Phase-compare Latch and the negative-going edge of -2F Early A (-2FEYA) resets it. The Phase-compare Latch issues a Phase-compare Latch Output (PCLO) signal to the Phase Comparator Charge Pump Circuit.

(5) Phase Comparator and Charge Pump

The Phase Comparator Charge Pump circuit issues a decrease frequency (DEC) signal when the VFO input phase is leading, and an increase frequency (INC) signal when the VFO input phase is lagging, comparing the phases between a DTIN2 signal and a PCLO signal.

The INC or DEC signal drives the constant-current circuit to charge or discharge the filter circuit (LP Fand Buffer).

(6) LPF and Buffer

The charge pump output is applied to a Low Pass Filter (LPF) and converted into DC voltage to control the VCO. During an initial seek operation or RTZ operation, the FLTSQ signal clamps the charge pump output to 0 V to recalibrate the VFO function.

During an initial data read operation, a VFO fast-sync (VFOFS) signal is issued to the VFO circuit which increases the loop gain of the VFO circuit to widen the pull-in range, and to shorten the pull-in time for synchronization to the RAWDT signal. At termination of the Data read operation, the same function is activated for synchronization with the PLO1F signal.

The LPF and Buffer output is applied to two stages of an emitter-follower circuit. It controls the VCO frequency as a control voltage (Vc) signal.

(7) VCO

The VCO circuit is an emitter-coupled multivibrator in which cross-coupled transistors, Q8 and Q9, form a positive-feedback gain stage. At any time either Q8 or Q9 and the timing capacitor, is alternately charged and discharged by the voltage-controlled current sources according to Vc signal.

The VCO circuit issues a 2F Early (2FEY) signal to the Data Separator and Write Compensation circuit. The 2FEY signal frequency increases when the Vc signal goes high, and decreases when Vc signal goes low.

(8) Data Separator

Through the before-mentioned process, the VFO circuit is synchronized with the RAWDT signal or PLO1F signal. The VCO output, 2FEY, is delayed to a -2F Late (2FLT) signal. The -2FLT signal is applied to the data window circuit and Data Sample circuit. The -2FLT signal is applied to two flip-flop in the Data window circuit, and then toggled at its positive-going edge. The VFO circuit can be synchronized with a normal phase relation or a 180 degree shifted phase relation. Therefore, the VFOFS and phase-adjust pulse (PADJP) signals function as a "0" during the VFO fast mode.

The data window circuit issues a VFO clock (VFOCLK) signal to the interface circuit and a data window (DTWD) signal to the Data Sample circuit.

The positive-going edge of the DLDT signal clocks the DTWD signal, and then issues a —separated data (—SPDT) signal. When VFOFS, PADJP and SPDT signals go true, the DTWD signal phase is changed to a "O" on the SPDT signal during VFO fast mode. The SPDT signal is clocked by the positive-going edge of the VFOCLK signal.

The timing chart of the VFO is shown in Figure 4-6-46, and the timing chart of the Data Separator is shown in Figure 4-6-47.

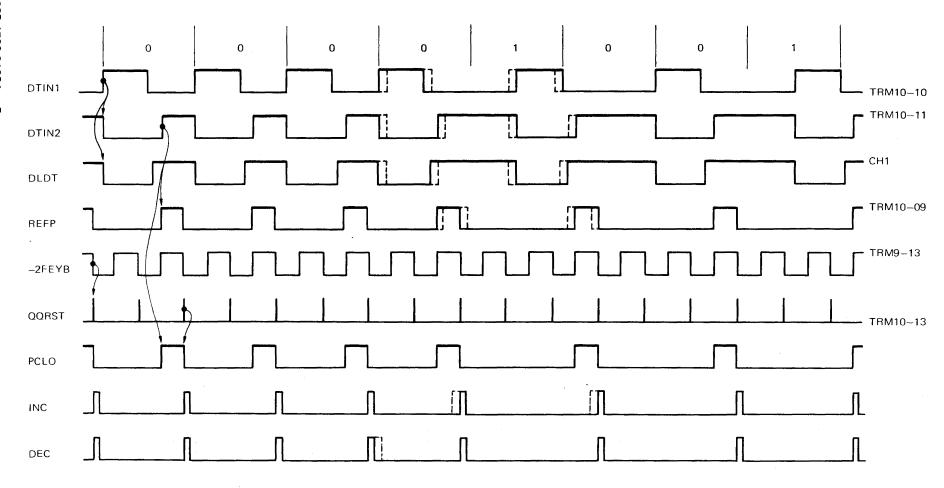


Figure 4-6-46 VFO Timing Chart

4.6.9.2 VFO Control Logic

The VFO control circuit controls the input to the VFO circuit; that is, the PLO output PLO1F or recovered read data, RAWDT, it also generates a VFO fast synchronization (VFOFS) signal for faster VFO synchronization with the input signals RAWDT or PLO1F.

In a start-up sequence, the leading edge of the PWRDY signal sets the FLTSQ signal to inhibit the input to the VFO circuit. The initial seek completion sets a Linear Mode (LNMD) signal, and then resets the FLTSQ signal to enable the synchronization of the VFO circuit. The leading edge of the FLTSQ signal clocks the initial VFO fast-sync (IVFOFS) counter which issues a 12-byte pulse of the IVFOFS signal and a 1-byte pulse of the Phase Adjust Pulse (PADJP) signal at the last of the IVFOFS signal.

The leading edge of the IVFOFS signal sets the Servo Mode (SVMD) latch. The SVMD signal is applied to the VFO input multiplexer so that the PLO1F signal is applied to the VFO. Simultaneously, the VFOFS signal (12-byte) activates the fast synchronization of the VFO circuit.

When either PWRDY or SPGD signal, go false or when a seek error has occurred, or when a RTZ command is issued to the drive, the FLTSQ signal will go true. A block diagram of VFO control is shown in Figure 4-6-48, and the timing chart of an initial VFO control is shown in Figure 4-6-49.

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Figure 4-6-48 VFO Control Logic Block Diagram

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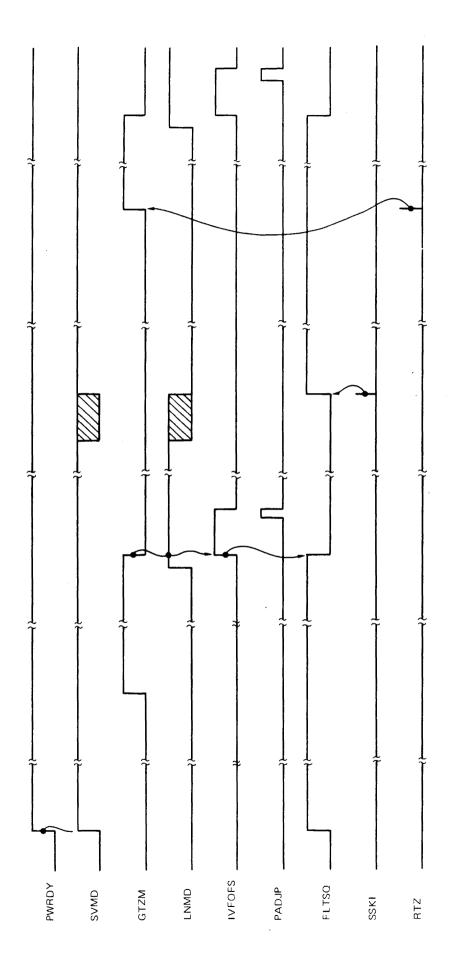


Figure 4-6-49 Initial VFO Control Timing Chart

During a Non-read operation, the VFO circuit synchronizes with the PLO output, PLO1F, and generates a VFO clock (VFOCLK). In Hard Sector mode, at the beginning of a read operation, Read Gate is applied to the RG True Detect circuit after 4 bits and is clocked by the negative-going edge of the Byte Clock (BYTCL) signal.

A rise read gate (RRG) signal, which is an output of the RG True Detect circuit, is applied to a 3 byte shift register. Its output then 12 on the lock-to-data counter to generate a 4-byte lock-to-data (LDATA) signal, and phase Adjust Pulse (PADJP). The leading edge of the LDATA signal resets Servo Mode (SVMD) so that the VFO circuit synchronizes with RAWDT.

In Variable Soft Sector Mode, the Rise AM Found (RAMF) signal sets the lock-to-data counter to generate the LDATA signal. (Refer to Figure 4-6-50).

At the end of the Read Gate signal, a one-byte Set Lock-To-PLO (SLPLO) signal is issued and applied to the Lock-To-PLO Counter to generate a 4-byte Lock To PLO (LPLO) signal. The LPLO signal sets Servo Mode (SVMD) so that the VFO circuit synchronizes with PLO1F.

The LDATA and LPLO signals are converted into the VFO Fast-sync (VOFS) signal-and applied to the VFO LPF circuit to decrease the time constant of the LPF. This promotes faster synchronization of the VFO circuit with RAWDT or PLO1F.

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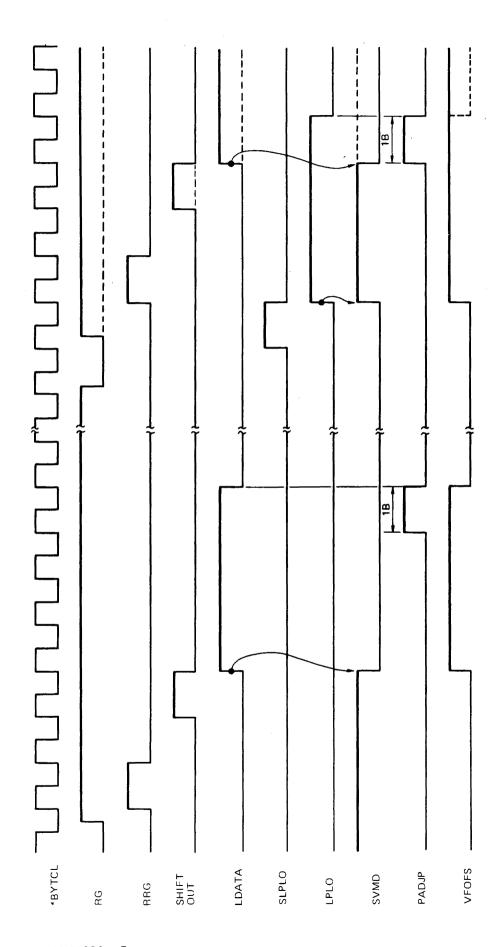


Figure 4-6-50 VFO Control Timing Chart

4.6.10 Fault and Error Detection

Faults and error except data fielding checks, are interpreted by the drive. These interpreted conditions are sent, via the interface, to the control unit and they are also displayed on fault indicator LEDs on the CNAN PCB.

4.6.10.1 Device Check

If an error sets the Device Check register, the Device Check (fault) line is enabled to the control unit, and the write circuit is inhibited.

Each of the six outputs of the device check register is designated as an unique statuses. If an optional Tag 5 function is enabled by the control unit, each Device Check status is enabled on the interface lives.

- (1) Control Check 1 (Status 0)
 - (A) URDY · (RG + WG + RTZ + TAG1 + OFST)
 - (B) (SKERR + UNSQ) · (TAG1 + OFST)
- (2) Control Check 2 (Status 1)
 - (A) WG·(RG + OFST + SKERR)
 - (B) RG·(WG + SKERR)
- (3) Read/Write Check 1 (Status 2)
 - (A) WG·(ONTRK + UNSQ)
 - (B) INTMOT
 - (C) VCMHT
 - (D) DMFL
- (4) Read/Write Check 2 (Status 3)

WG-UNSF

(5) Read/Write Check 3 (Status 4)

WG-FPT

(6) Read/Write Check 4 (Status 5)

(WG + RG)·MLTSL

The Device Check register and each status is cleared by pressing the Check Clear key on the optional operator panel or by enabling the Device Check (Fault) Clear signal from the control unit.

4.6.10.2 Seek Check (Seek Error)

If a seek malfunction has occurred in the drive, the malfunction will set the Seek Check latch and enable the Seek Error (SKERR) line to the control unit. Each of the output of the Seek Check latch output is designated unique Seek Check statuses.

- (1) Time Out (TMOT)
- (2) Seek on Guard Band (SEKGB)
- (3) Linear Mode on Guard Band (LNMGB)
- (4) RTZ on Outer Guard Band (RTOGB)
- (5) Over-shoot Check (OVSHT)
- (6) Illegal Cylinder Address (ILCYL)

4.6.10.3 Fault Indicator

The Not-Ready status, Device Check Status and Seek Check status outputs (15 status lives) are applied to a priority encoder circuit and then converted into four lines which drives the fault indicator LEDs as shown in Table 4-6-3.

Table 4-6-3 Fault Indicators

Hex Code	Fault	Priority	
1	DC Motor Fault (DMFL)	Highest	
2	VCM Over-heat (VCMHT)		
3	Initial Seek Time-out (INTMOT)		
4	Control Check 1 (CTCK1)		
5	Control Check 2 (CTCK2)		
6	Read/Write Check 1 (RWCK1)		
7	Read/Write Check 2 (RWCK2)		
8	Read/Write Check 3 (RWCK3)		
9	Read/Write Check 4 (RWCK4)		
А	Time-out (TMOT)		
В	Seek Guard on Guard Band (SEKGB)		
С	Linear Mode Guard Band (LNMGB)		
D	RTZ on Outer Guard Band (RTOGB)		
E	Over-shoot Check (OVSHT)		
F	Illegal Cylinder Address (ILCYL)	Lowest	

Section 5 **Troubleshooting Guide**

5. TROUBLESHOOTING GUIDE

5.1 INTRODUCTION

This section will contain troubleshooting flow charts according to the error status on the disk unit and control unit.

Note: Before any operation is attempted, maintenance personnel should read carefully Section 6 (Maintenance) and fully understand the details of the procedures and tools required.

Check the eleven items in the following list before applying power to the unit.

- (1) Ensure that the AC line conditions satisfy the power supply requirements.
- (2) Ensure that the DC voltages satisfy the unit requirement.
- (3) Inspect the interface cables to ensure pin 1 on the cable goes to pin 1 of the connect or at both the unit and at the control unit.
- (4) If the unit is in a daisy chain mode with one or more units, make sure that only the last unit has a line terminator (LTN) installed.
- (5) Ensure that the actuator lock is in the "OFF" position.
- (6) Ensure that the desired logical unit number (LUN) of the unit is selected on the CNAM PCB, see Section 3.7.1 and that each LUN in the system is unique.
- (7) Ensure that Hard/Soft sector mode is selected, see Section 3.7.2, per the system configuration.
- (8) In the case of Hard Sector (fixed sector length), ensure that the correct sector count is set on CNAM PCB, see Section 3.7.6.
- (9) Ensure that Tag 4/5 Enable or Disable per is set, see Section 3.7.3 the system configuration.
- (10) Ensure that File Protect key is on the proper position to meet the system requirement, see Section 3.7.4.
- (11) Ensure that Disable/Normal keys are correctly set to the Normal position.
- (12) Ensure the Release Timer key is set to the desired position.
- (13) Ensure that all PCB assemblies and cables are firmly seated.

5.2 ERROR STATUS

The disk unit, optional power supply unit (PSU), and/or the control unit will issue the following statuses as shown in Table 5-2-1.

Table 5-2-1 Error Status

Error Status	Definition	Information Source	
Alarm	Power malfunction has occurred on the disk unit or optional PSU.	Optional PSU	
Not Selected	The control unit cannot select the specified disk unit.	Disk Unit Control Unit	
Not Power Ready (*PWRDY)	DC power is not sufficient for the specified voltage.	Disk Unit (CMZM)	
Not Speed Good (*SPGD)	The rotational speed is not within 3,600 rpm $\pm 6\%$.	Disk Unit (CMZM)	
Device Check (DVCK)	DVCK indicates a fault condition has occurred in the disk unit.	Disk Unit (CNAM)	
Seek Error (SKERR)	SKERR status indicates that a seek malfunction has occurred in the disk unit.	Disk Unit (CNAM) Control Unit	
Read Error	READ ERROR status result if a data error has occurred in read operation.	Control Unit	
AM Missing	AM MISSING status indicates the Address Mark (AM) has not been found in a AM read operation. (Soft sector mode)		
Dual Channel	DUAL CHANNEL malfunction concerns Select/Reserve functions. Control Uni		

Maintenance personnel can see the Device Check or Seek Error status at Fault Indicator LEDs on CNAM PCB assembly, and Not Power Ready and Not Speed Good statuses on CMZM PCB assembly. The Seek Error or Device Check status is defined by ST8 to ST1 LEDs as shown in Table 5-2-2.

Table 5-2-2 Fault Indicator Definition

Error Status	Status Bit				F Code	Dosaviation	
	ST8	ST4	ST2	ST1	Error Code	Description	
Device Check (Fault)	0	0	0	1	1	DC Motor Fault	(DMFL)
	0	0	1	0	2	VCM Heat	(VCMHT)
	0	0	1	1	3	Initial Seek Time-out	(INTMOT)
	0	1	0	0	4	Control Check 1	(CTCK1)
	0	1	0	1	5	Control Check 2	(CTCK2)
	0	1	1	0	6	Read/Write Check 1	(RWCK1)
	0	1	1	1	7	Read/Write Check 2	(RWCK2)
	1	0	0	0	8	Read/Write Check 3	(RWCK3)
	1	0	0	1	9	Read/Write Check 4	(RWCK4)
Seek Error	1	0	1	0	Α	Time-out	(TMOT)
	1	0	1	1	В	Seek on Guard Band	(SEKGB)
	1	1	0	0	С	Linear Mode on Guard Band	(LNMGB)
	1	1	0	1	D	RTZ on Outer Guard Band	(RTOGB)
	1	1	1	0	E	Over-shoot Check	(OVSHT)
	1	1	1	1	F	Illegal Cylinder Address	(ILCYL)

5.3 TROUBLESHOOTING SYMBOL

The troubleshooting flow charts contain the procedures beginning with an error status, to pursure trouble sources.

The following conventions are provided to aid understanding the symbols used in this trouble shooting flow charts as shown in Table 5-3-1.

Table 5-3-1 Symbol of Flow Chart

Symbol	Description	
	Terminals. Starting point of the trouble.	
	Decision, go ahead according with YES or NO. (Reference test point.)	
	Connector, go ahead same-numbered symbol in same sheet.	
\Box	Connector, go ahead same-numbered symbol in another sheet.	
	Process, perform activity given.	

5.4 TROUBLESHOOTING FLOW CHART

In this paragraph, the following flow charts are provided.

Figure 5-4-1	Alarm
Figure 5-4-2	Not Selected
Figure 5-4-3	Not Power Ready
Figure 5-4-4	Not Speed Good
Figure 5-4-5	Device Check
Figure 5-4-6	Seek Error
Figure 5-4-7	Read Error
Figure 5-4-8	AM Missing
Figure 5-4-9	Dual Channel

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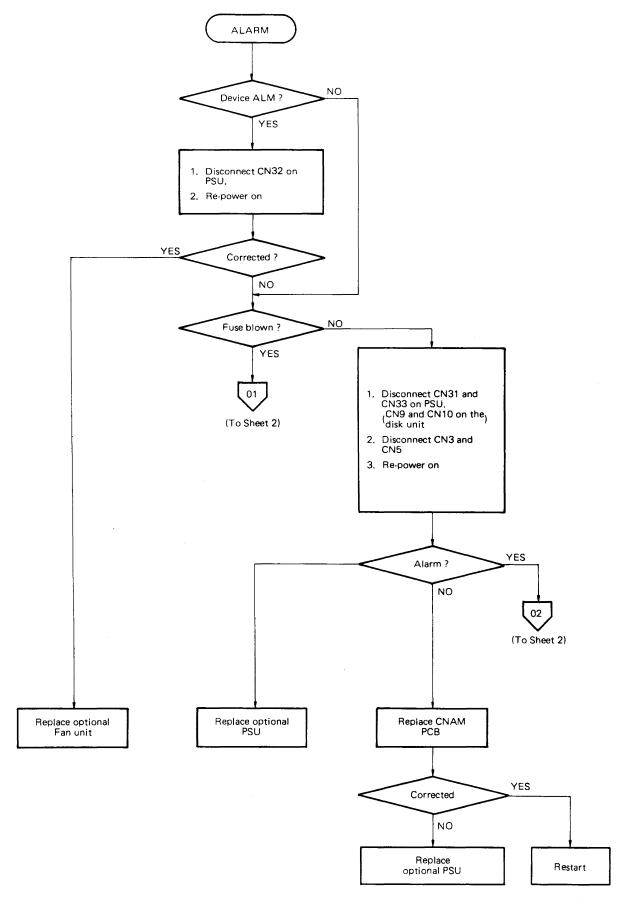


Figure 5-4-1 Alarm Flow Chart (Sheet 1 of 2)

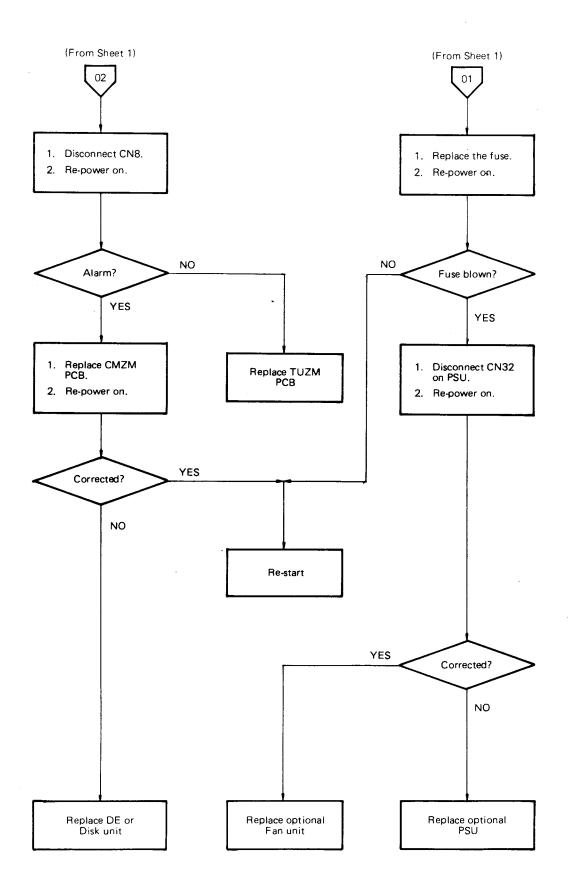


Figure 5-4-1 Alarm Flow Chart (Sheet 2 of 2)

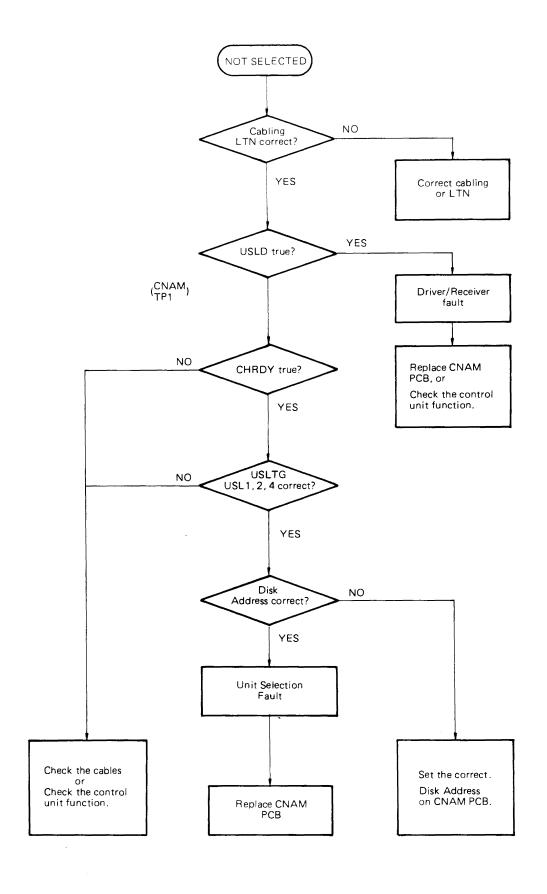


Figure 5-4-2 Not Selected Flow Chart

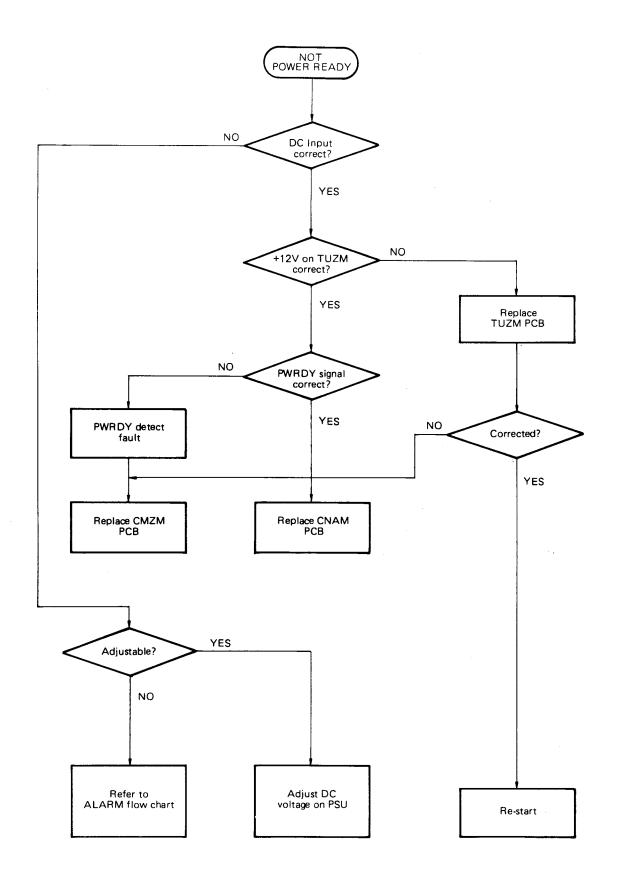


Figure 5-4-3 Not Power Ready Flow Chart

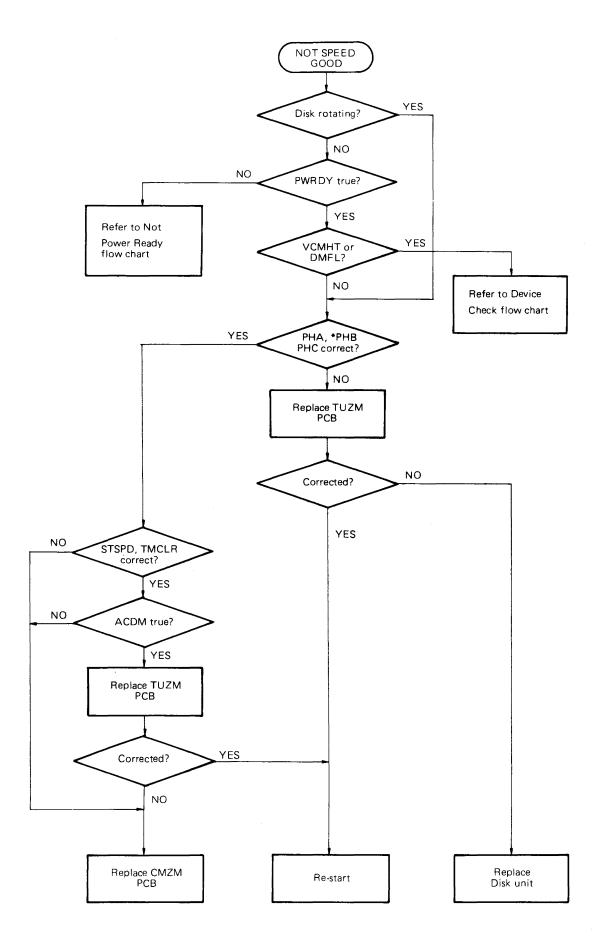


Figure 5-4-4 Not Speed Good Flow Chart

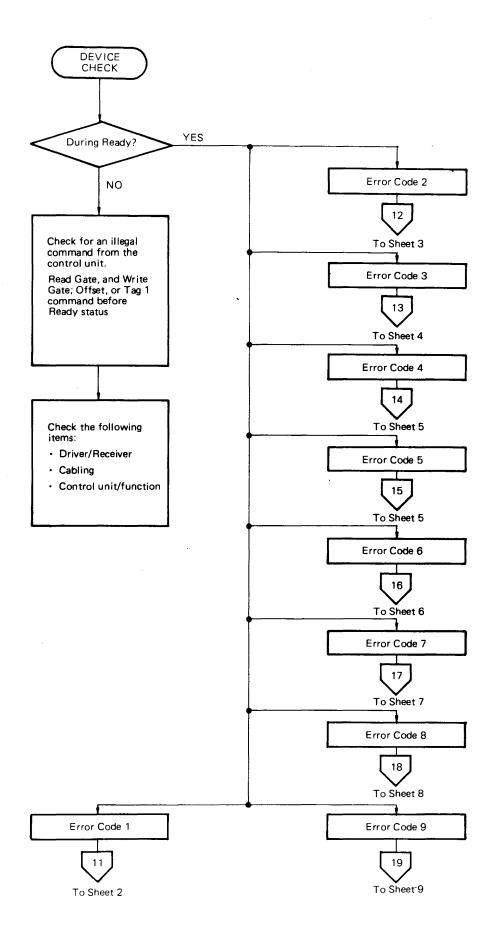


Figure 5-4-5 Device Check Flow Chart (Sheet 1 of 9)

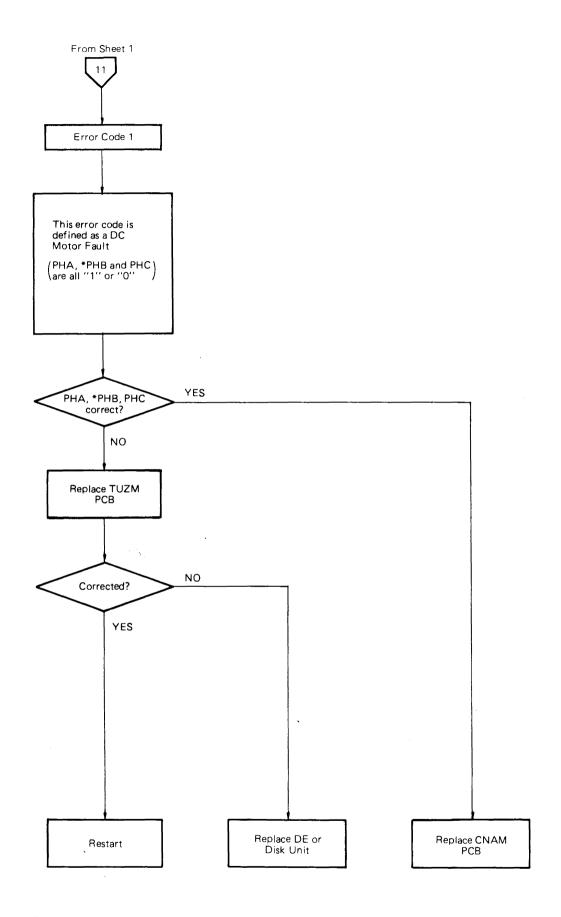


Figure 5-4-5 Device Check Flow Chart (Sheet 2 of 9)

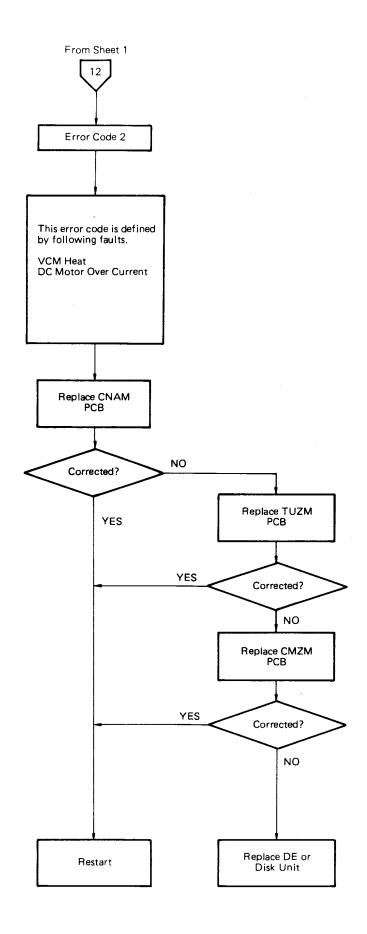


Figure 5-4-5 Device Check Flow Chart (Sheet 3 of 9)

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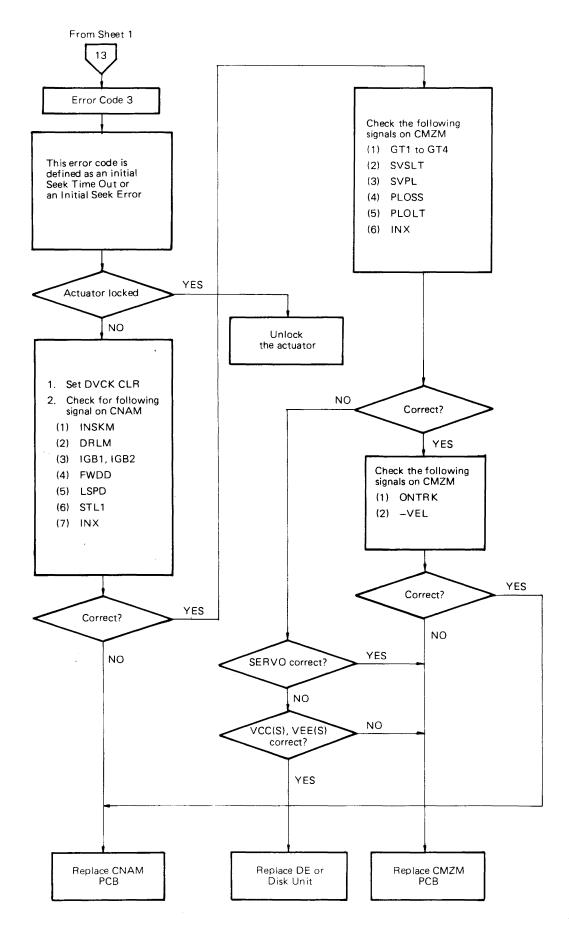


Figure 5-4-5 Device Check Flow Chart (Sheet 4 of 9)

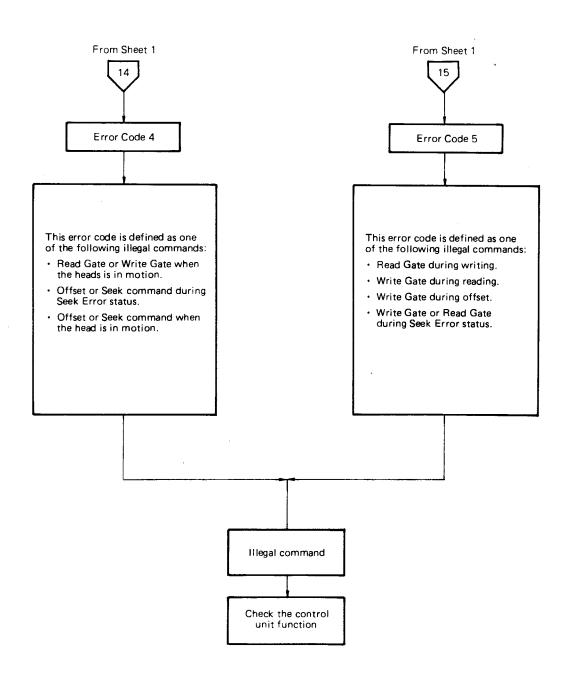


Figure 5-4-5 Device Check Flow Chart (Sheet 5 of 9)

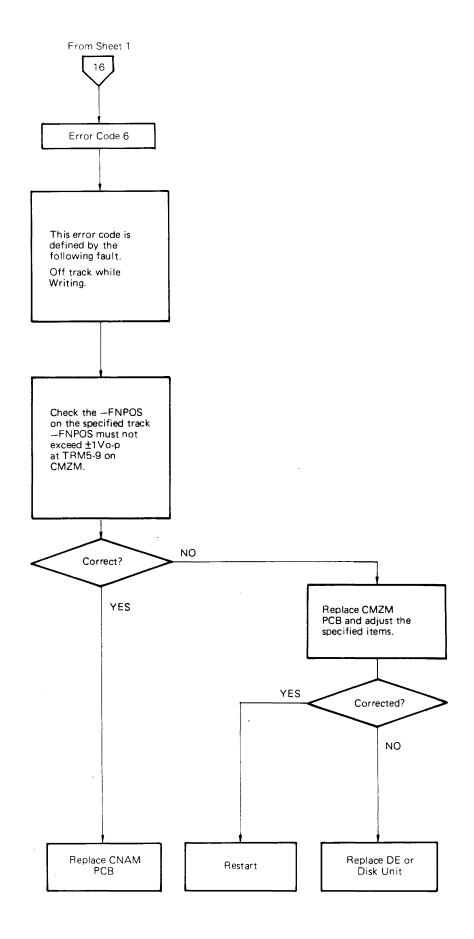


Figure 5-4-5 Device Check Flow Chart (Sheet 6 of 9)

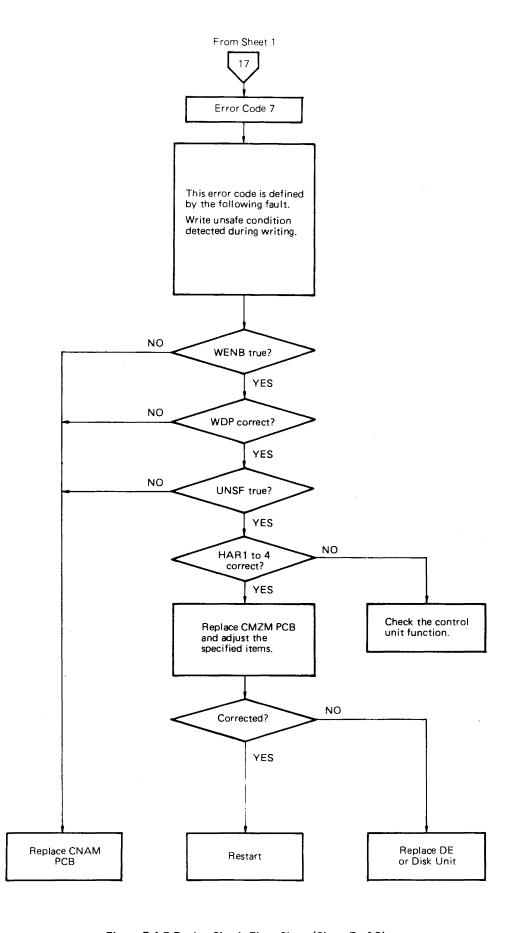
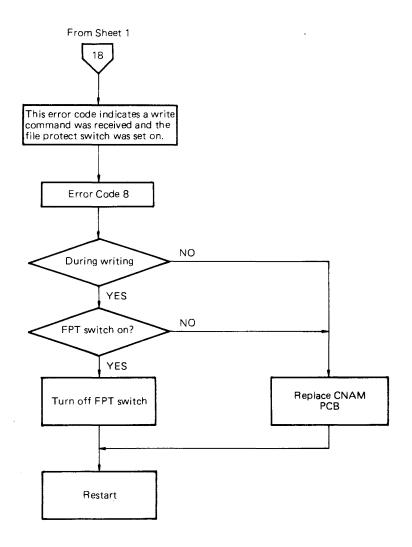


Figure 5-4-5 Device Check Flow Chart (Sheet 7 of 9)



Note: FPT (file-protect) switches are located on the front panel and the CNAM PCB assembly.

Figure 5-4-5 Device Check Flow Chart (Sheet 8 of 9)

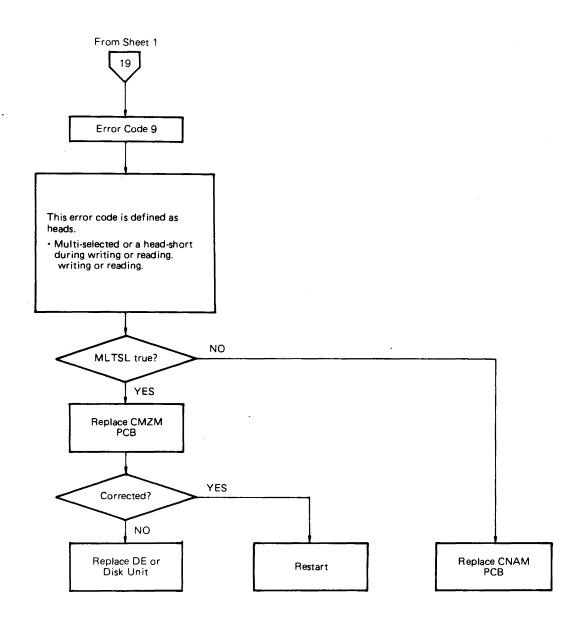


Figure 5-4-5 Device Check Flow Chart (Sheet 9 of 9)

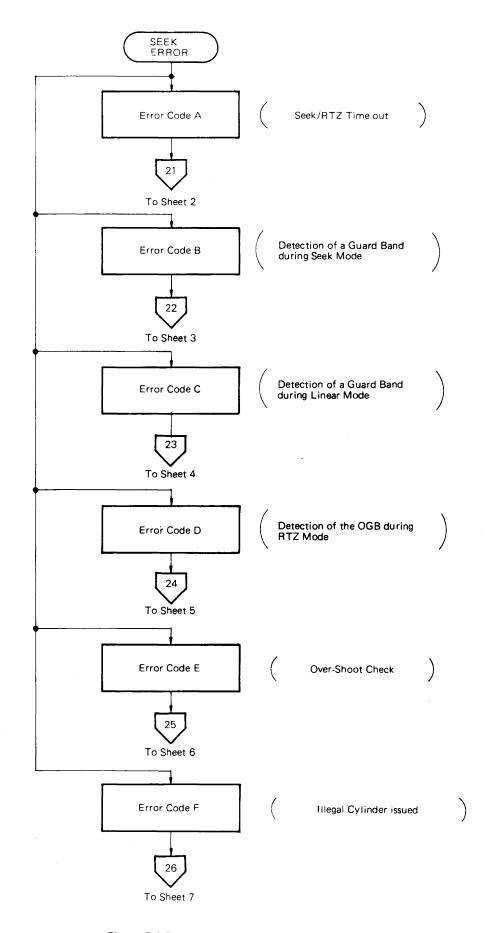


Figure 5-4-6 Seek Error Flow Chart (Sheet 1 of 7)

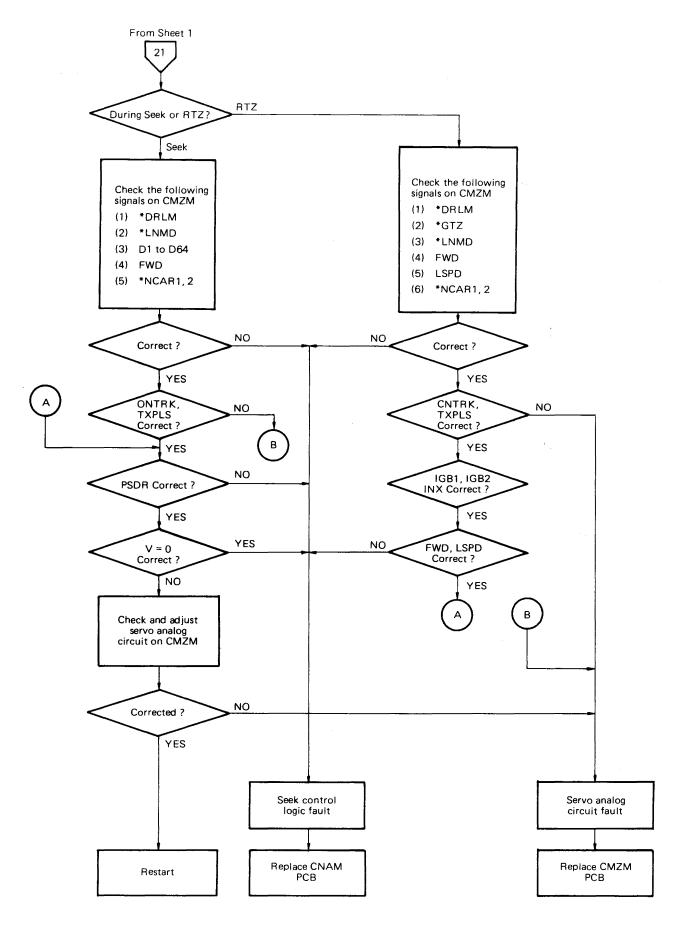


Figure 5-4-6 Seek Error Flow Chart (Sheet 2 of 7)

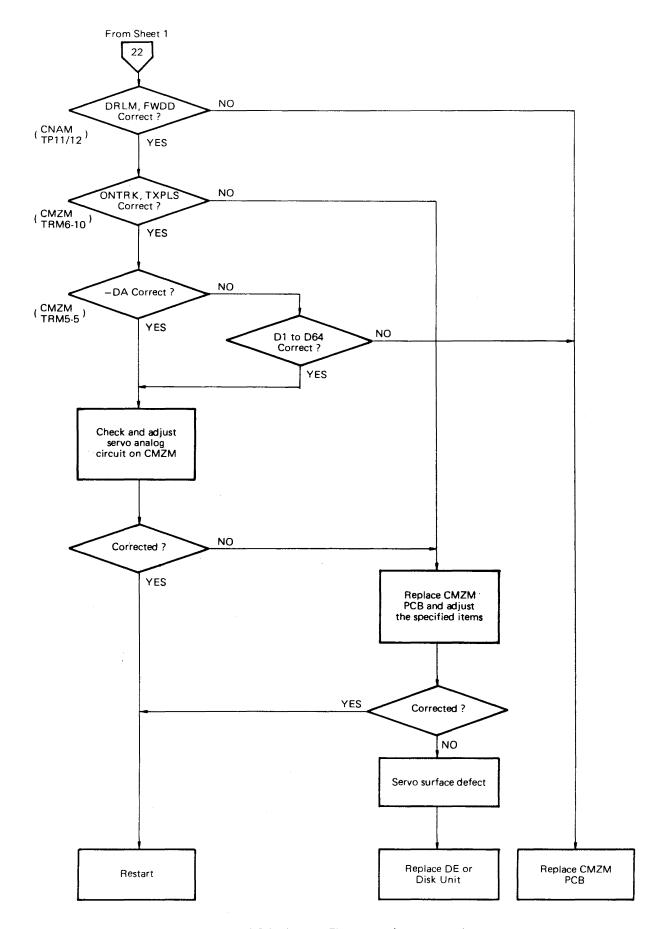


Figure 5-4-6 Seek Error Flow Chart (Sheet 3 of 7)

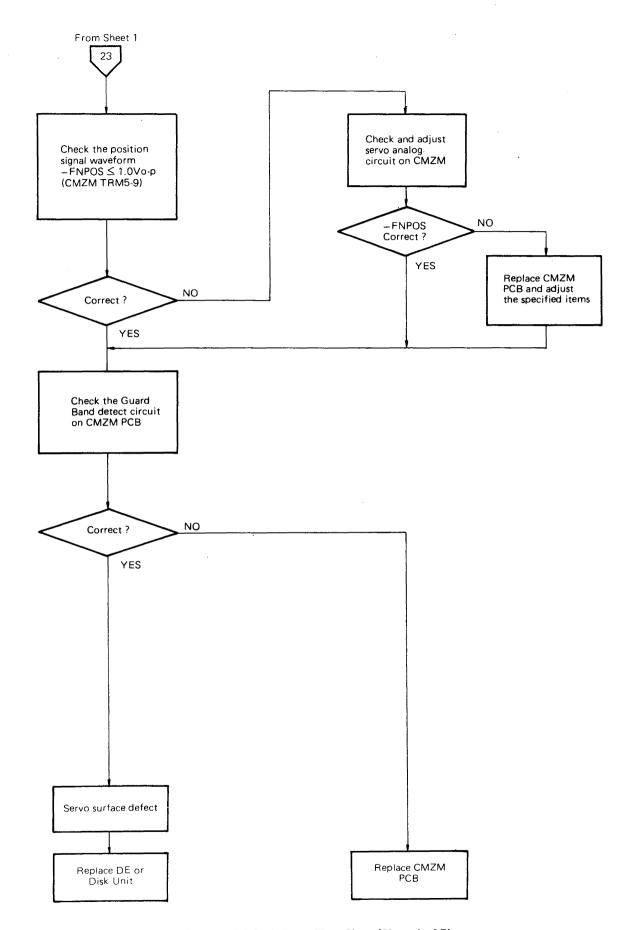


Figure 5-4-6 Seek Error Flow Chart (Sheet 4 of 7)

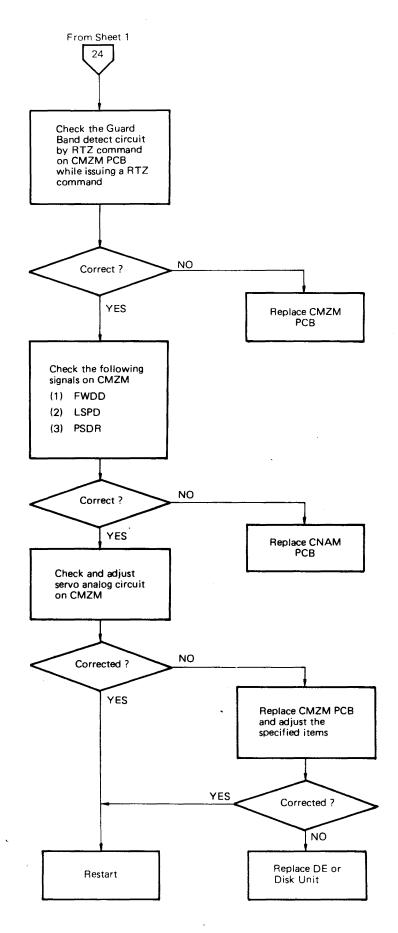


Figure 5-4-6 Seek Error Flow Chart (Sheet 5 of 7)

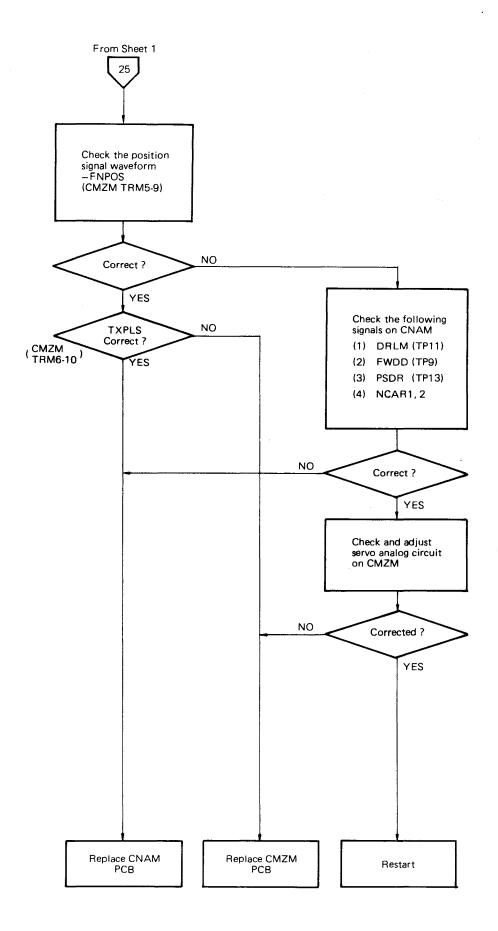


Figure 5-4-6 Seek Error Flow Chart (Sheet 6 of 7)

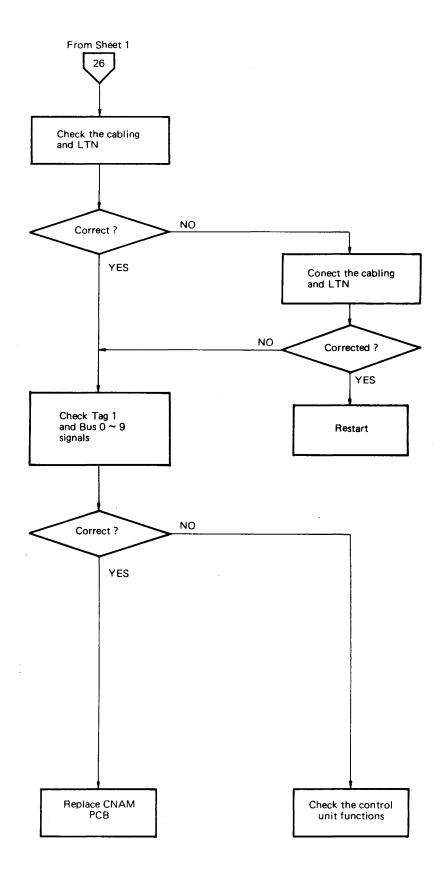
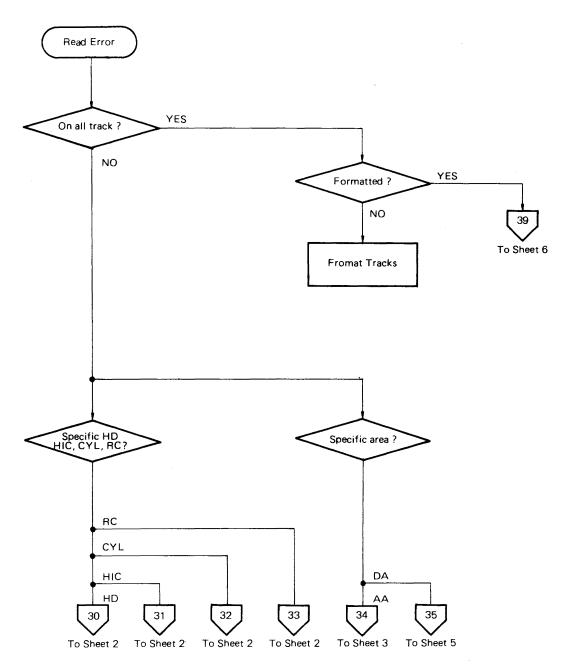


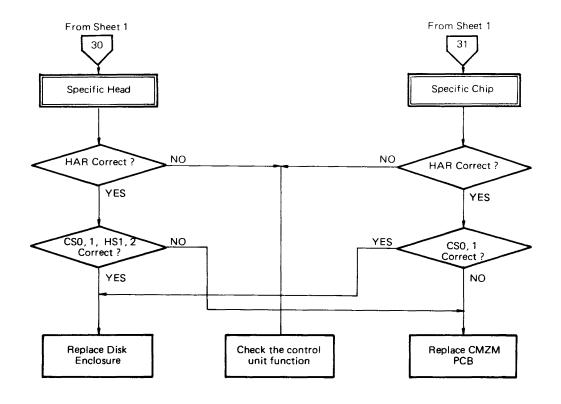
Figure 5-4-6 Seek Error Flow Chart (Sheet 7 of 7)

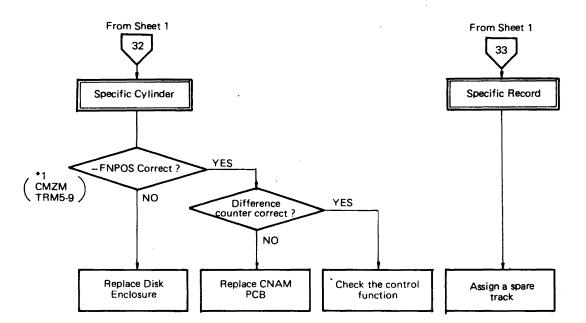


Note: 1) AA is Address Area

2) DA is Data Area.

Figure 5-4-7 Read Error Flow Chart (Sheet 1 of 6)





Note: 1) If the noise exceeding 1.0Vo-p appears on -FNPOS signal during Linear Mode, it is incorrect.

2) One HIC chip has four/three heads.

CS0: HD0 to 3 CS1: HD4 to 6

Figure 5-4-7 Read Error Flow Chart (Sheet 2 of 6)

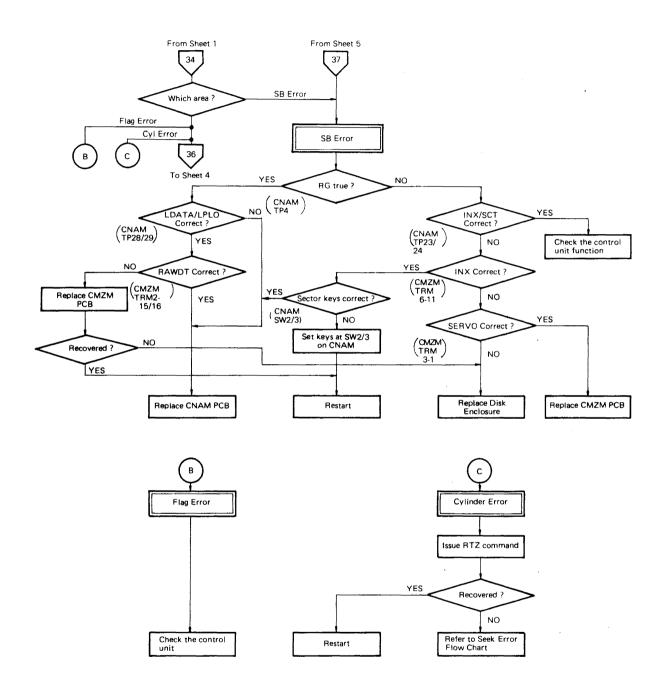


Figure 5-4-7 Read Error Flow Chart (Sheet 3 of 6)

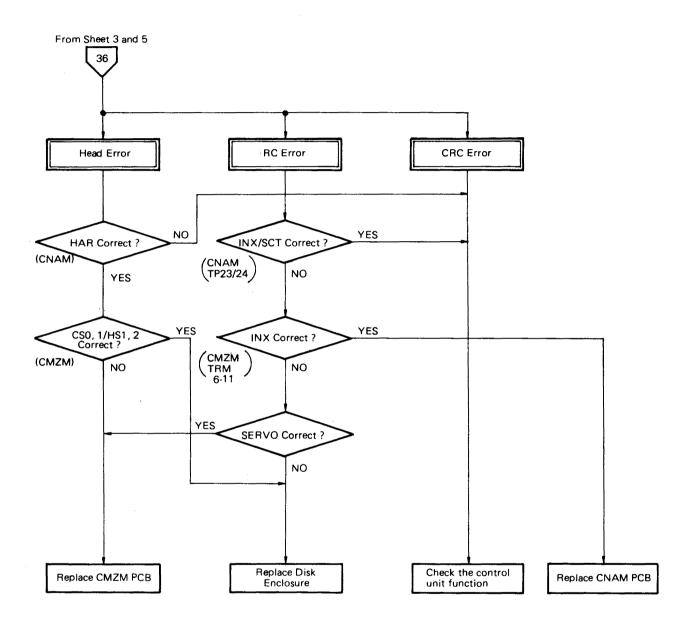


Figure 5-4-7 Read Error Flow Chart (Sheet 4 of 6)

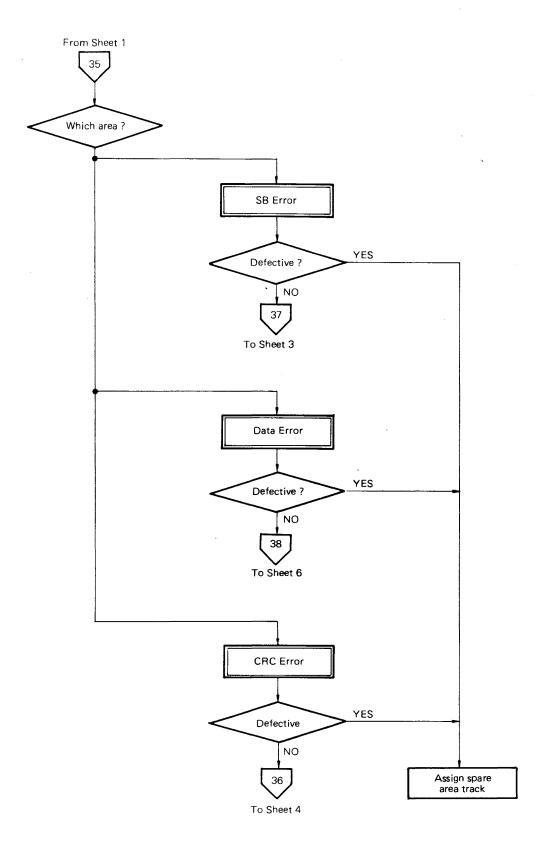


Figure 5-4-7 Read Error Flow Chart (Sheet 5 of 6)

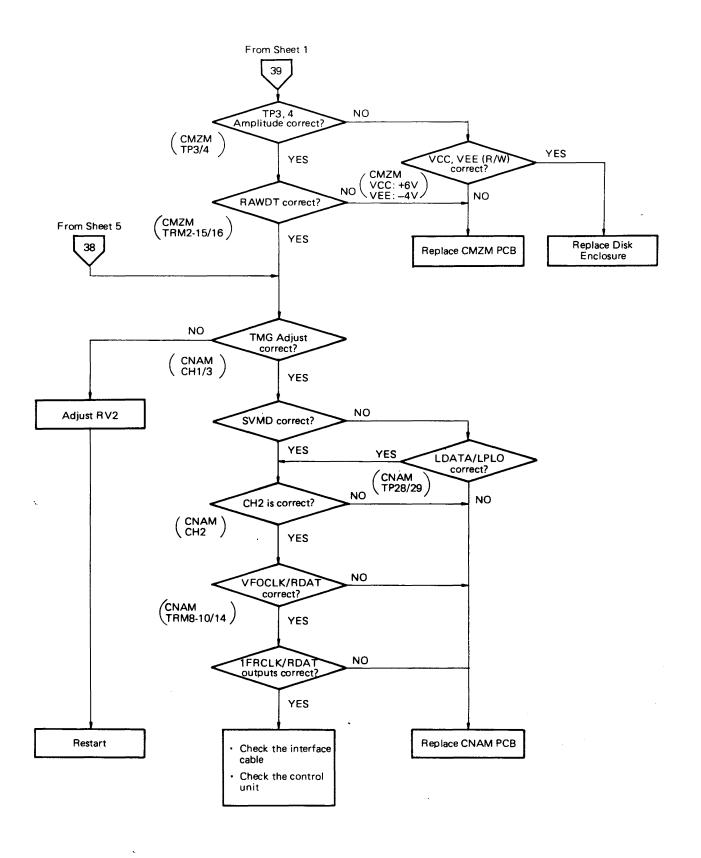


Figure 5-4-7 Read Error Flow Chart (Sheet 6 of 6)

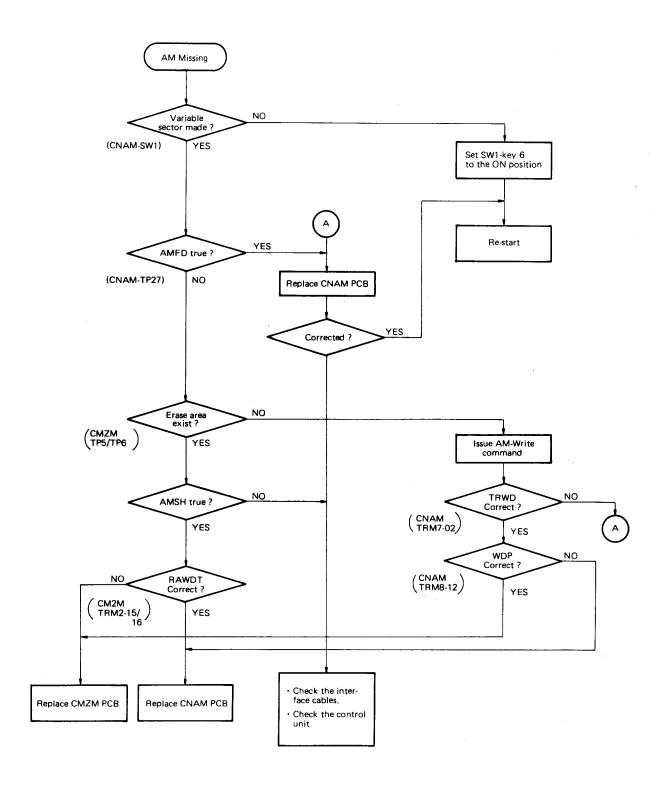


Figure 5-4-8 AM Missing Flow Chart

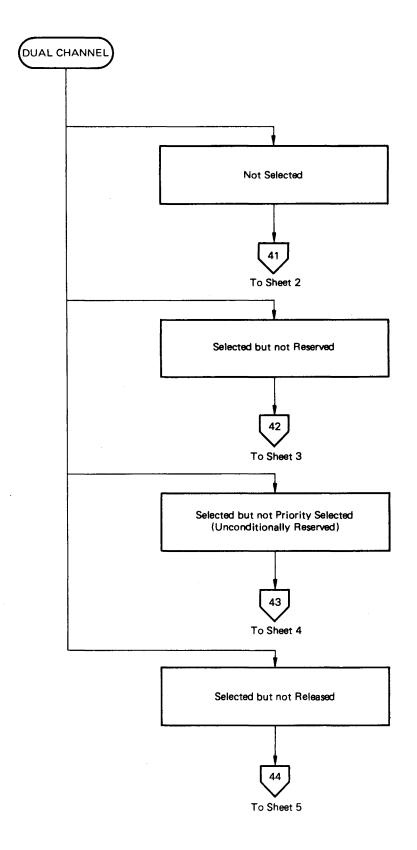


Figure 5-4-9 Dual Channel Malfunction Flow Chart (Sheet 1 of 5)

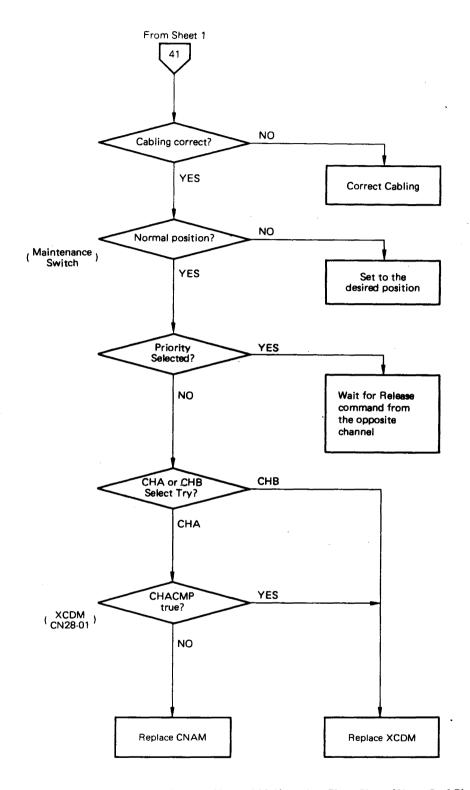


Figure 5-4-9 Dual Channel Malfunction Flow Chart (Sheet 2 of 5)

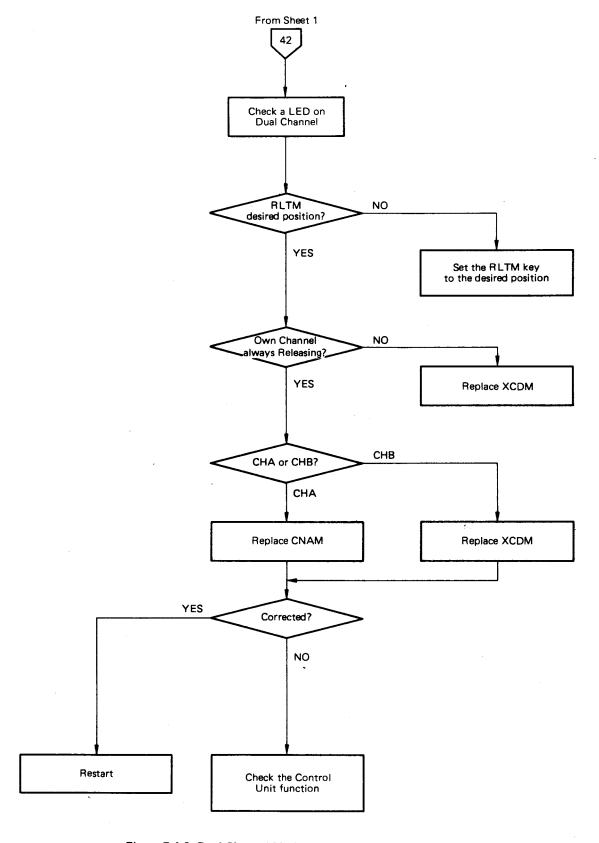


Figure 5-4-9 Dual Channel Malfunction Flow Chart (Sheet 3 of 5)

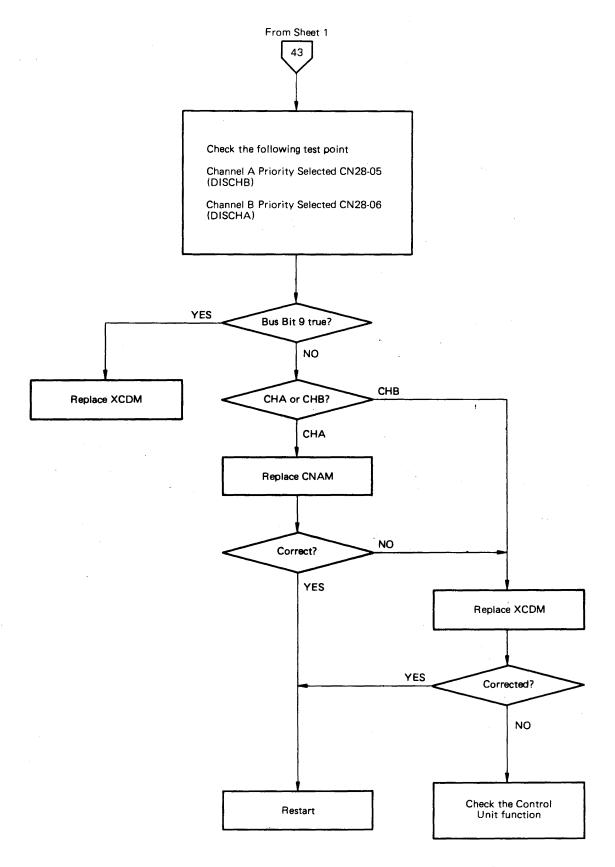


Figure 5-4-9 Dual Channel Malfunction Flow Chart (Sheet 4 of 5)

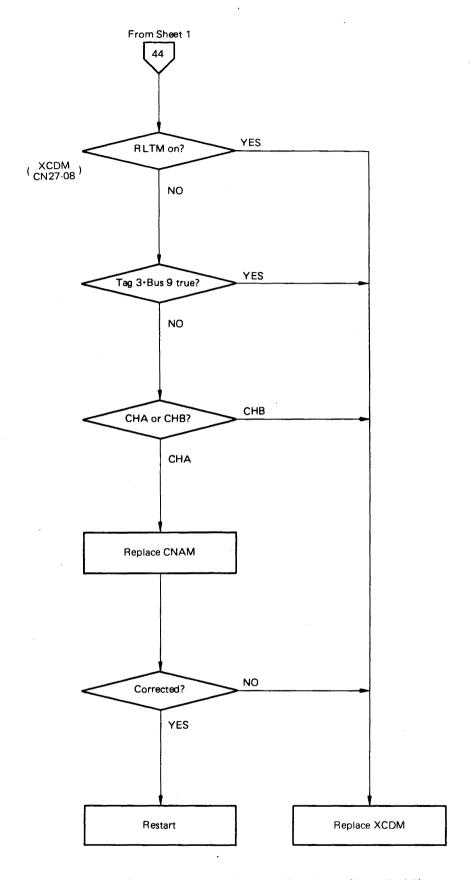


Figure 5-4-9 Dual Channel Malfunction Flow Chart (Sheet 5 of 5)

Section 6 Maintenance

6. MAINTENANCE

6.1 INTRODUCTION

This section covers maintenance of the unit, and is divided into General Precautions, Preventive Maintenance, Maintenance Equipment, Parts Replacement, and Electrical Checks and Adjustment items.

6.2 GENERAL PRECAUTIONS

6.2.1 Power On/Off

- (1) Visually check the condition of the device before turning the power on or off.
- (2) Always turn the power off before removing or inserting printed circuit boards or connectors.
- (3) After maintenance, before turning the power on, ensure that all printed circuit boards and connectors correctly seated and installed in the correct position.

6.2.2 Parts Replacement

- (1) Use screwdrivers that match the size of the screws.
- (2) Do not leave removed screws in the drive.

Caution: Never loosen the retaining clamps for the DE plastic cover. The DE must not be opened in the field. Screws marked with paint on their heads must not be loosened.

6.2.3 Dual Channel Switches

- (1) Turn the switches to the desired position according to system configura-
- (2) After maintenance, turn the maintenance switch to the Normal A/B (NRA/NRB) position.

6.2.4 Other

- (1) Use test equipment that has been correctly calibrated.
- (2) Always record failure symptoms and remedies employed for later reference.

6.3 MAINTENANCE TOOLS AND EQUIPMENT

Table 6-3-1 Maintenance Tools and Equipment

Tool and equipment	Model
Oscilloscope	TEKTRONIX 475, or equivalent
Oscilloscope probe (x 10)	TEKTRONIX P6053B, or equivalent
Digital multimeter	
Screwdriver	

6.4 PREVENTIVE MAINTENANCE

No preventive maintenance is required.

6.5 PCB ASSEMBLY REPLACEMENT

The parts required for maintenance are the three printed circuit board assemblies. (Refer to Section 7. Spare Parts.) This section describes the removal of bad PCB.

6.5.1 PCB Assembly Arrangement

Three PCB assemblies are mounted on the DE as shown in Figure 6-5-1.

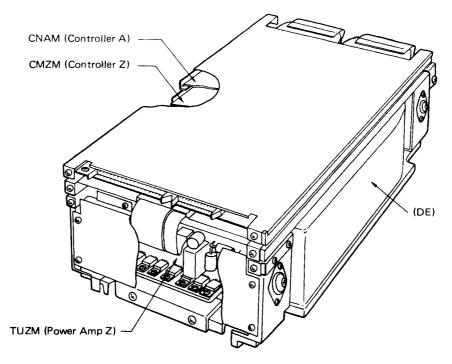


Figure 6-5-1 PCB Assy. Arrangement

6.5.2 CNAM PCB Assembly Replacement Procedure

Refer to Figure 6-5-2.

To replace the CNAM PCB Assembly, proceed as follows:

- (1) Removal
 - (A) Loosen screws "A" and remove the top cover.
 - (B) Disconnect wiring (CN3 and CN4) from the CMZM PCB assembly.
 - (C) Remove the six screws indicates in Figure 6-5-2.
 - (D) Remove the CNAM PCB assembly by lifting it.
- (2) Installation
 - (A) Fasten the CNAM PCB Assembly to the side frame, six screws.
 - (B) Fasten connectors (CN3 and CN4).
 - (C) Install the top cover and tighten screws "A".

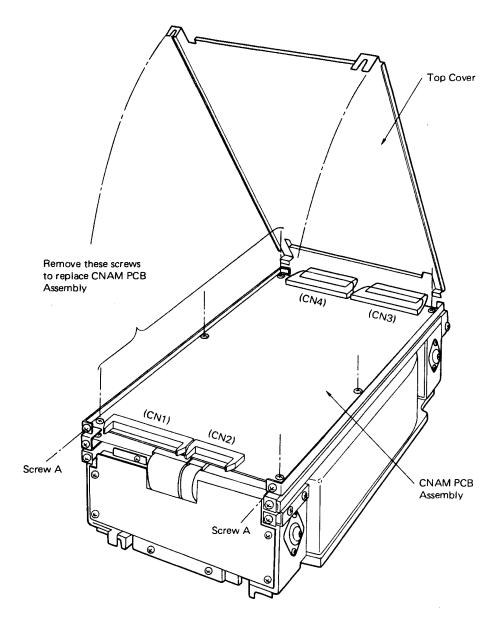


Figure 6-5-2 CNAM PCB Assembly Replacement

6.5.3 CMZM PCB Assy. Replacement Procedure

To replace the CMZM PCB Assembly, proceed as follows: Refer to Figure 6-5-3.

- (1) Removal
 - (A) Loosen screws "B".
 - (B) Rise the CNAM PCB Assy. by lifting up the upper side-frame. The upper side-frame is held with a pivot on one end, and can be raised more than 90°.
 - (C) Loosen screw "C" and remove the upper side-frame support, illustrated in Figure 6-5-3.In this condition the component on the CMZM can be checked.
 - (D) Disconnect wiring (CN5, CN6, CN7, CN8, CN9, and CN10).

(E) Remove six screws, and lift out the CMZM PCB Assembly. Be careful not to damage the CN15 on the TINM (Through Connector). The TINM is connected to the CMZM PCB assembly at the back of the board. Refer to Figure 6-5-4. CN15 will be disconnected by lifting the CMZM PCB assembly.

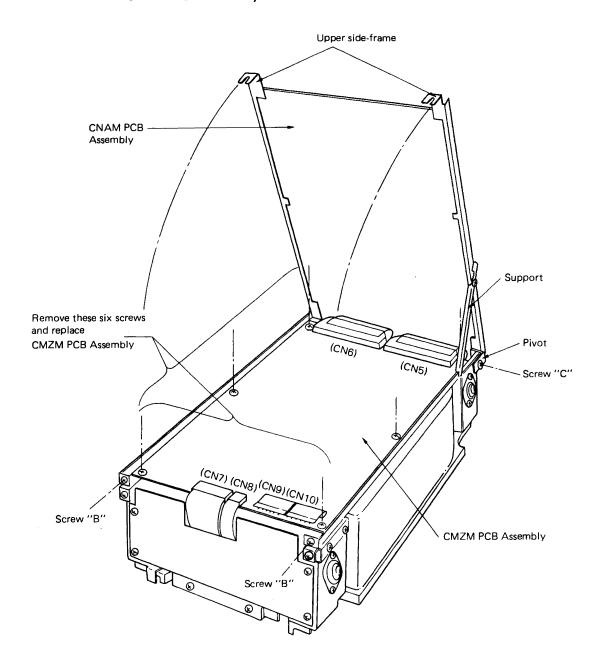
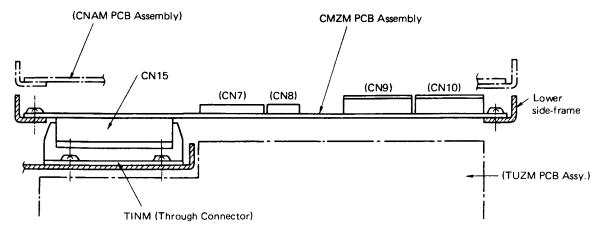


Figure 6-5-3 CMZM PCB Assembly Replacement



(Back view from rear side)

Figure 6-5-4 TINM Connection

(2) Installation

- (A) Set the CMZM PCB assembly on the lower side-frame. Then, check that CN15 is connected correctly.
- (B) Fasten the six screws, and fasten other connectors.
- (C) Restore the upper side frame support and close the CNAM PCB assembly with the upper side-frame, to its original position tighten screws "C".
- (D) Tighten screws "B".

6.5.4 TUZM PCB Assembly Replacement

The TUZM PCB assembly is mounted on the rear side of DE. Refer to Figure 6.5.5.

(1) Removal

- (A) Remove the Fan Unit (which is optional) or the cover by removing the the screws "D".
- (B) Disconnect wiring (CN11, CN12, CN13, and CN14) from the DE and the CMZM PCB assembly.
- (C) Remove screws "E".

Note: Be careful not to lose the isolating bushings, which bit around the threaded portion of the screws "E". When replacing the TUZM PCB assembly.

(2) Installation

- (A) Fasten the TUZM PCB assembly to the DE as illustrated in Figure 6-5-5.
- (B) Fasten connectors coming from the DE and the CMZM PCB assembly.
- (C) Install the optional Fan Unit or the cover.

6.5.5 XCDM PCB Assembly Replacement

The XCDM PCB assembly is a component of Dual Channel option, and commonly used for two types of Dual Channel option which is mounted on the optional power supply unit or on the upper portion of the drive.

The XCDM PCB assembly replacement procedure is as follows.

(1) Removal

- (A) Remove two screws fixing the protect cover.
- (B) Remove the protect cover.
- (C) Disconnect the connectors CN21 to CN25, and also disconnect the IC socket cables S1 to S4.
- (D) Pushing the PCB assembly, pull it up.
- (E) Remove XCDM PCB assembly by removing four screws from the mounting frame.

(2) Installation

- (A) Fasten the XCDM PCB assembly by four screws to the mounting frame.
- (B) Pushing the PCB assembly, pull it down.
- (C) Connect the cables to connectors CN21 to CN25 and IC sockets S1 to S4.
- (D) Mount the cover.
- (E) Fasten two screws to fix the cover.

Note: The procedure is common for two types of Dual Channel option.

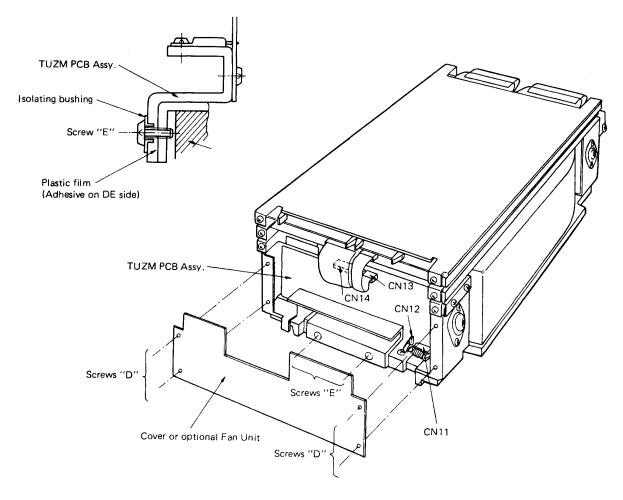


Figure 6-5-5 TUZM PCB Assembly Replacement

6.6 PCB CHECK AND ADJUSTMENT

6.6.1 Test Point Arrangement on PCB

Each PCB assembly is provided with test points and potentiometers to check and/or adjust circuit functions.

(1) CNAM PCB assembly

The test points and potentiometers are located on the CNAM PCB assembly as shown in Figure 6-6-1. Test points are listed in Table 6-6-1, check terminals in Table 6-6-2, potentiometers in Table 6-6-3, and switch keys in Table 6-6-4.

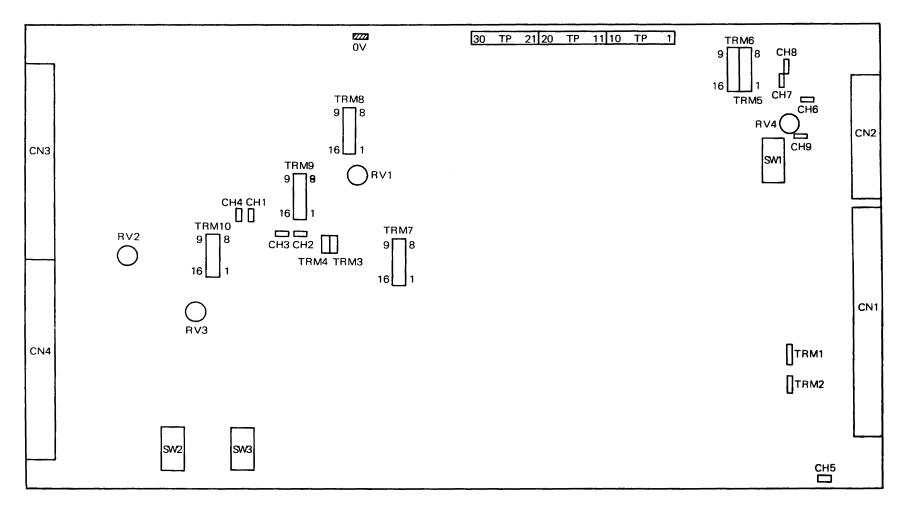


Figure 6-6-1 CNAM PCB Assembly Test Points

Table 6-6-1 CNAM Test Points

TP No.	Abbreviation	Signal Name	Signal Level	Schematic Code
1	СНАСМР	Channel A Compare	TTL	AC1
2	*CHAENB	Channel A Enable	TTL	AC1
3	WG	Write Gate	TTL	AD1
4	RG	Read Gate	TTL	AD1
5	INSKM	Initial Seek Mode	TTL	AE1
6	GTZM	Go To Zero Mode	TTL	AE1
7	SEKM	Seek Mode	TTL	AE1
8	*UNSQ	Under Sequence	TTL	AE1
9	FWDD	Forward Drive	TTL	AE2
10	0 V	Ground		
11	DRLM	Drive Linear Motor	TTL	AE2
12	LNMD	Linear Mode	TTL	AE2
13	PSDR	Position Drive	TTL	AE2
14	LSPD	Low Speed	TTL	AE2
15	SKC	Seek Complete	TTL	AF1
16	RDY	Ready	TTL	AF1
17	SKERR	Seek Error	TTL	AF1
18	ONCYL	On Cylinder	TTL	AF1
19	SKEND	Seek End	TTL	AF1
20	0 V	Ground		
21	ТМОТР	Time Out Pulse	TTL	AG1
22	D=0	Difference Equal to Zero	TTL	AH2
23	*INX	Index	TTL	AJ1
24	*SCT	Sector	TTL	AJ1
25	DVCK	Device Check	TTL	AL2
26	*AMRD	AM Read	TTL	AM1
27	AMFD	AM Found	TTL	AM1
28	LDATA	Lock to Data	TTL	AM1
29	LPLO	Lock to PLO	TTL	AM1
30	0∨	Ground		
CH1	DLDT	Delayed Data	ECL	AN1
2	VFOVC	VFO Control Voltage	Analog	AN2
3	DTWD	Data Window	ECL	AP1
4	-5.2 V	-5.2 V DC (VFO)	DC	AP1
5	–5 V	-5 V DC	DC	AB2
6	STL1	Settling 1	TTL	AF1
7	STL2	Settling 2	TTL	AF1
8	INHWCK	Inhibit Write Check	TTL	AL1
9	STL3	Settling 3	TTL	AF1

Table 6-6-2 CNAM Check Terminals

		TRM5	(G4 right)		
Pin	ABBR	Signal Name	Pin	ABBR	Signal Name
09	0 V	Ground	08	0 V	Ground
10	(*STL3)		07	(*STL3)	
11	(OFST)		06	(OFST)	-
12	(*STL2)		05	(*STL2)	
13	(NOSEK)		04	(NOSEK)	-
14	(*STL3)		03	(*STL3)	4
15	(MS2)		02	(MS2)	4
16	(MS1)		01	(MS1)	4
		TRM6	(G4 left)	-	
Pin	ABBR	Signal Name	Pin	ABBR	Signal Name
09	0 V	Ground	08	0 V	Ground
10			07		
11			06		
12			05		
13	(SCT)		04	(SCT)	-
14	(INX)		03	(INX)	-
15	(TRWDD)		02	(TRWDD)	
16	(TRWD)		01	(TRWD)	-
		TRM	7 (D18)		
Pin	ABBR	Signal Name	Pin	ABBR	Signal Name
09	(SVMD)		08	(SVMD)	
10	(SYCGT)		07	(SYNGT)	
11	(WDAT)		06	(WDAT)	-
12	0 V	Ground	05	0 V	Ground
13	(*VFOFS)		04	(*VFOFS)	
14	(*FLTSQ)		03	(*FLTSQ)	-
15	(*TRWD)		02	(*TRWD)	
16	(*PADJP)		01	(*PADJP)	

Note) The pins shown by " \rightarrow \leftarrow " must be connected with short-plug (C63L-0790-0001).

Table 6-6-2 CNAM Check Terminals (Continued)

		TRM	3 (F20)		
Pin	ABBR	Signal Name	Pin	ABBR	Signal Name
09	(VFOCLK)		08	(VFOCLK)	•
10	RCLK	Read Clock	07		
11	0V	Ground	06		
12	*WDP	Write Data Pulse	05		
13	(RDAT)		04	(RDAT)	-
14	RDAT	Read Data	03		
15			02		
16	(RAWDT)		01	(RAWDT)	-
		TRM	(E22)		
Pin	ABBR	Signal Name	Pin	ABBR	Signal Name
09	VFOFS	VFO Fast Sync	08	0 V	Ground
10	FLTSQ	Filter Squelch	07	0 V	Ground
11	PHRST	Phase Reset	06	0 V	Ground
12	-2FOT	2F On-Time	05	0 V	Ground
13	-2FEYB	2F Early B	04	0 V	Ground
14	WCL2	Write Clock 2	03	0 V	Ground
15	-2FLT	2F Late	02	0 V	Ground
16	SYCK	Sync Clock	01	0 V	Ground
		TRM1	0 (D25)		
Pin	ABBR	Signal Name	Pin	ABBR	Signal Name
09	REFP	Reference Pulse	08	WDT2	Write Data 2
10	DTIN1	Data In 1	07	0 V	Ground
11	DTIN2	Data In 2	06	0 V	Ground
12	-INC	Increase	05	0 V	Ground
13	QQRST	QQ Reset	04	o v	Ground
14	+DEC	Decrease	03	0 V	Ground
15	-DEC	Decrease	02	0 V	Ground
16	+INC	Increase	01	0 V	Ground

Note) The pins shown by " \rightarrow \leftarrow " must be connected with short plug (C63L-0790-0001).

Table 6-6-3 CNAM Potentiometer Function

Pot. No.	Function/Adjustment	Reference TP
RV1	VFO Free-run Frequency	CH2/TRM9-13
2	Time-margin Measurement	CH1/CH3
3	Reference Pulse Width Adjustment	TRM10-9
4	Settling 1 (2.5 ms)	СН6

Note: No adjustment is required on any potentiometer when the CNAM PCB is replaced.

Table 6-6-4 CNAM Switch Function

No.	Function	Reference TP
SW1	Disk Addressing Device Type (when Tag 4/5 enabled) Tag 4/5 Enable Hard/Soft Sector mode File Protect	None
SW2 SW3	Sector Counting	TP23/TP24
TRM1 TRM2	Busy signal terminator	None
TRM3 TRM4	VCO (VFO) select	CH2/TRM9-13

(2) CMZM PCB assembly

The test points and potentiometers located on the CMZM PCB assembly are shown in Figure 6-6-2. Test points are listed in Table 6-6-5, potentiometers in Table 6-6-6 switches in Table 6-6-7. Three LEDs are located on the CMZM PCB assembly as follows:

ACDM (Orange): indicates that accelerate mode is activated.

SPGD (Orange): indicates that the rotational speed is within ±6% of the

nominal value.

PWRDY (Green): indicates that +5 V, -12 V, +24 V and internal +12 V are

within the nominal voltage.

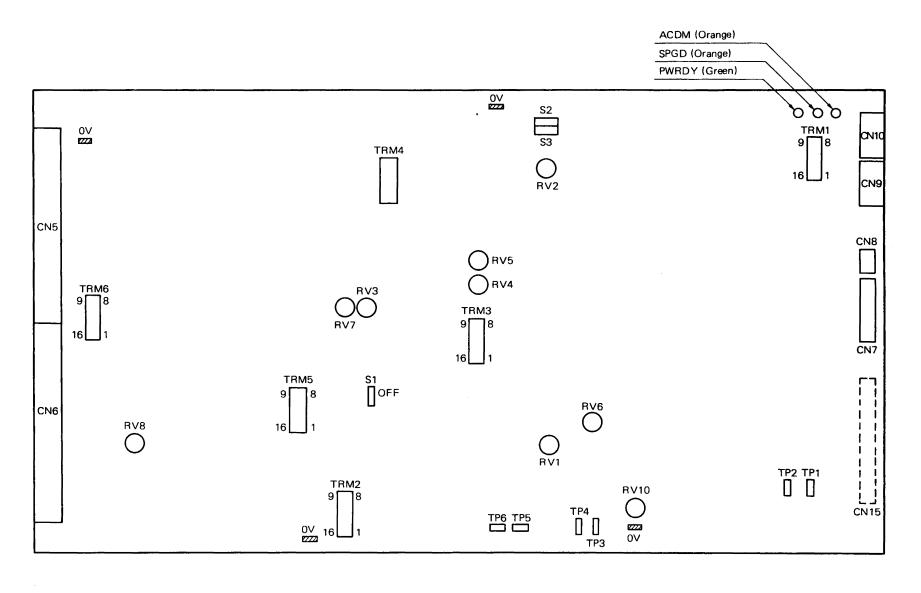


Figure 6-6-2 CMZM PCB Assembly Test Points

Table 6-6-5 CMZM Test Points

No.	Abbreviation	Signal Name	Signal Level	Schematic Code
TP1	WCA	Write Current A	Analog	BD1
2	WCB	Write Current B Analog		BD1
3	PROT1	Pre-amplifier Output 1	Analog	BD2
4	PROT2	Pre-amplifier Output 2	Analog	BD2
5	AGCOT1	AGC Output 1	Analog	BD2
6	AGCOT2	AGC Output 2	Analog	BD2
TRM1- 1	PHA	Phase A	TTL	BB1
2	*PHB	Phase B	TTL	BB1
3	PHC	Phase C	TTL	BB1
4	-			
5	-			
6	_			
7	_			
8	_			
9				
10	*CTCL1	Control Clock 1	TTL	BB2
11	TEST	Test (test purpose only)	TTL	BC1
12	_			
13	Q44	Q44	TTL	
14	*STARTP	Start Pulse	TTL	BB1
15	*TMCLK	Timer Clock	TTL	BB1
16	STSPD	Set Speed	TTL	881
TRM2- 1	*DIGLT	Diag Latch (test purpose only)	TTL	BD1
2	PLSH1	Pulse Shaper 1	ECL	BD2
3	PLSH2	Pulse Shaper 2	ECL	BD2
4	SMPCK	Sample Clock	ECL	BD2
5	INTLT1	Integrator Latch 1	ECL	BD2
6	INTLT2	Integrator Latch 2	ECL	BD2
7	DIFOT1	Differentiator Output 1	ECL	BD2
8	DIFOT2	Differentiator Output 2	ECL	BD2
9	UNSF	Unsafe	ECL	BD1
10	MLTSL	Multi-Selected	ECL	BE1
11	0 V	Ground		
12	0 V	Ground		
13	0 V	Ground		
14	0 V	Ground		
15	-RAWDT	Raw Data	ECL	BD2
		, arr pata		J 502

Table 6-6-5 CMZM Test Points (Continued)

No.	Abbreviation	Signal Name	Signal Level	Schematic Code
TRM3- 1	SERVO	Servo Signal	Analog	BF1
2	AGC	AGC Voltage	Analog	BG1
3	CSNS	Current Sense	Analog	вн3
4	PLOSS	PLO Single-shot	TTL	BF1
5	*HDLD	Head Loaded	TTL	BG1
6	PLOLT	PLO Latch	TTL	BF1
7	POSN	Position Normal	Analog	BG1
8	0 V	Ground		
9	POSQ	Position Quadruture	Analog	BG1
10	SVPWD	Servo Pulse Window	TTL	BG1
11	TESTP	Test Point (test Purpose only)	TTL	BF1
12	SVPLS	Servo Pulse	TTL	BF1
13				
14	-ABSVL	Absolute Velocity	Analog	вн1
15	SVSLT	Servo Slice Out	TTL	BF1
16	CLP	Clamp (test purpose only)	TTL	BF1
TRM4- 1	PLO1F	PLO 1 Frequency	TTL	BF2
2	*GT1	Gate 1	TTL	BF2
3	*GT2	Gate 2	TTL	BF2
4	*GT3	Gate 3	TTL	BF2
5	BYTCLK	Byte Clock	TTL	BF2
6	_			
7	PLOVC	PLO Control Voltage	TTL	BF2
8	0 V	Ground		
9	*MSDT	Missing Detect	TTL	BF2
10	_			
11	*GT4	Gate 4	TTL	BF2
12	IGB2P	IGB2 Pulse	TTL	BF2
13	_			
14	OGBP	OGB Pulse	TTL	BF2
15	IGB1P	IGB1 Pulse	TTL	BF2
16	RAWINX	Raw Index	TTL	BF2

Table 6-6-5 CMZM Test Points (Continued)

No.	Abbreviation	Signal Name	Signal Level	Schematic Code
TRM5- 1	PADR	Power Amplifier Drive	Analog	внз
2	-VEL	Velocity	Analog	BH1
3	-			
4	-			
5	-DA	Digital To Analog Output	Analog	BH2
6	-			
7	CLPOS	Clamp Position	Analog	BH2
8	0 V	Ground		
9	-FNPOS	Fine Position	Analog	BH1
10	_			
11	_			
12	_			
13	PER	Position Error	Analog	вн2
14	VER	Velocity Error	Analog	BH2
15				
16	FUNC	Function	Analog	BH2
TRM6- 1	*OFTRK	Off Track	TTL	BG1
2	N+Q>0	POSN + POSQ > 0	TTL	BG1
3	N>Q	POSN > POSQ	TTL	BG1
4	_			
5	*OGB	OGB	TTL	BF3
6	_			
7	DRLM	Drive Linear Motor	TTL	ВН4
8	0 V	Ground		
9	FWDD	Forward Drive	TTL	BH4
10	TXPL	Track Crossing Pulse	TTL	вн4
11	*INX	Index	TTL	BF2
12	*IGB2	IGB2	TTL	BF3
13	*IGB1	IGB1	TTL	BF3
14	-			
15	V=0	Velocity Equal to Zero	TTL	BH1
16	ONTRK	On Track	TTL	BG1

Table 6-6-6 CMZM Potentiometer Function

Pot. No.	Function/Adjustment	Reference TP
RV1	Read Amplifier Offset Adjustment	TP5/TP6
2	VCO (PLO) Adjustment	TRM4-7/TRM4-1
3	Positioning Time Adjustment*	CNAM-TP15
4	Servo Pulse Window Adjustment	TRM3-10
5	PLOSS Adjustment	TRM3-4
6	Position Signal Gain Adjustment*	TRM3-7/TRM3-9
7	Velocity Offset Adjustment	TRM5-2
8	DAC Output Adjustment	TRM5-5
10	Write Current Adjustment	TP1/TP2

Note) Adjust potentiometers RV3 and RV6 when the CMZM PCB assembly is replaced.

Table 6-6-7 CMZM Switch Function

No.	Function	Reference TP
S1	Power Amplifier Drive Cut	,
S2 S3	VCO (PLO) Adjustment	TRM4-7/TRM4-1

(3) XCDM PCB Assembly

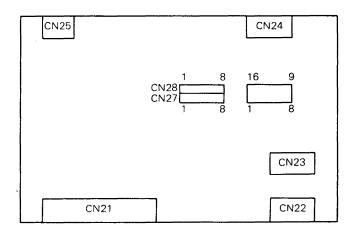


Figure 6-6-3 XCDM PCB Assembly Test Points

Table 6-6-8 XCDM Test Points

	CN27 (E9)			CN28 (E9)		
Pin	ABBR	Signal Name	Pin	ABBR	Signal Name	
1	CHAENB	Channel A Enable	1	СНАСМР	Channel A Compare	
2	DISAK	Disable A Key	2	*DISCHB2	Disable Channel B2	
3	DISAB	Disable B Key	3	BUSYB	Busy B	
4	*CHASLD	Channel A Selected	4	PWRDY	Power Ready	
5	CHBENB	Channel B Enable	5	DISCHB	Disable Channel B	
6	*CHBSLD	Channel B Selected	6	DISCHA	Disable Channel A	
7	*DISCHA2	Disable Channel A2	7	SKENDA	Seek End A	
8	RSTMK	Release Timer Key	8	SKENDB	Seek End B	
		CN2	9 (F9)			
Pin	ABBR	Signal Name	Pin	ABBR	Signal Name	
1	*INTR	Interrupt	16	*INTR	←	
2	*RSTMP	Release Timer Pulse	15	*RSTMP	←	
3	СНВСМР	Channel B Compare	14	BUSYA	Busy A	
4	CLK1	Clock 1	13	CLK1	←	
5	*RSVCL	Reserve Clock	12	*RSVCL	←	
6	CHARSV	Channel A Reserved	11	CHBRSV	Channel B Reserved	
7	CLK2	Clock 2	10	CLK2	←	
8	RSTMP	Release Timer Pulse	9	RSTMP	←	

6.6.2 PCB Adjustment and Selection after PCB Replacement

Refer to Table 6-6-9 for the required adjustments and selections when a PCB assembly is replaced.

Table 6-6-9 Adjustments and Selections after PCB Replacement

item	Spare Part	Adjustment/Selection
1	TUZM (B16B-7640-0010A)	None
2	CMZM (B16B-6960-0010A)	(1) Position Signal Gain Adjustment (RV6) (2) Positioning Time Adjustment (RV3)
3	CNAM (B16B-6970-0010A) (Refer to 3.7)	 (1) Disk Addressing (SW1) (2) Sector Mode (SW1) (3) Tag 4/5 Enable (SW1) (4) File Protect (SW1) (5) Device Type (SW1) (6) Sector Counting (SW2/SW3)

6.6.2.1 Position Signal Gain Adjustment

- (1) Confirm that the drive has normal status.
- (2) Repeatedly issue a alternate seek command between Cylinder 0 and Cylinder 192 (decimal).
- (3) Connect the test point TRM6-7 (DRLM) to one vertical input channel of an oscilloscope and trigger with the positive-going edge of the signal on the CMZM PCB (DC coupled).
- (4) Connect test point TRM3-7 (POSN) to the other vertical input channel of the oscilloscope (DC coupled).
- (5) Adjust potentiometer RV6 so that the POSN signal amplitude is 8.0 V ±0.4 V (peak-to-peak). Refer to Figure 6-6-4.

Note: For a coarse adjustment, issue a RTZ command and adjust potentiometer RV7 according to item (5).

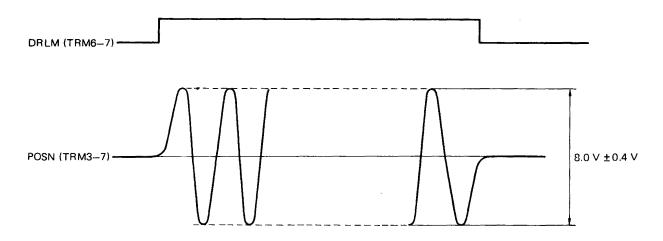


Figure 6-6-4 Position Signal Gain Adjustment

6.6.2.2 Positioning Time Adjustment

- (1) Repeat the procedure given in Section 6.6.2.1 item (1) through (3).
- (2) Connect test point TRM5-5 (-DA) to the other vertical input channel of the oscilloscope (DC coupled).
- (3) Adjust potentiometer RV3 so that decelerate time (Tdc) is $9.0 \text{ ms} \pm 0.4 \text{ ms}$.

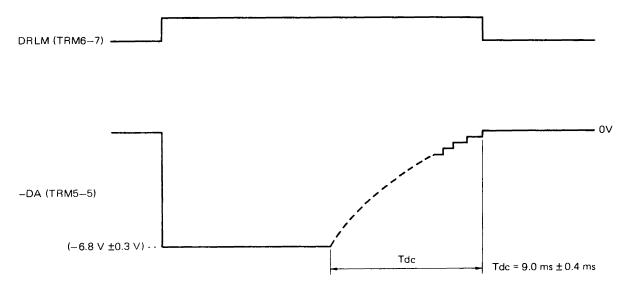


Figure 6-6-5 Positioning Time Adjustment

6.6.3 Electrical Measurement

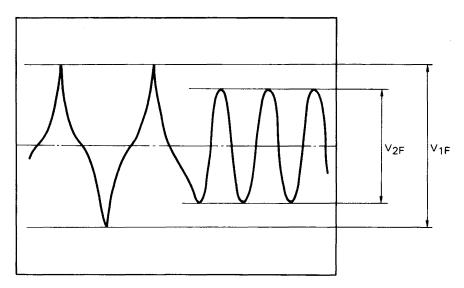
This section describes electrical measurements.

6.6.3.1 Read Output Measurement

Caution

Use the 0 V terminals near test points TP3 and TP4 on the CMZM PCB, and use a 200 MHz wide band pass oscilloscope. Measurement error may occur if these precautions are not followed.

- (1) Confirm that the specific track can be rewritten for the Read Output measurement.
- (2) Write repetitive "10" pattern (all "A₁₆") to all records on the specific track, e.g. CE track or Cylinder 0 track.
- (3) Connect test points TP3 and TP4 on the CMZM PCB with differential mode (inverted CH2 and add with CH1).
- (4) After writing, measure the pead-to-peak level V₂F and V₁F as shown in Figure 6-6-6.



 $V_{2F} \ge 200 \text{ mVp-p}$ Resolution Ratio = $\frac{V_{2F}}{V_{1F}} \times 100(\%) \ge 55\%$

Figure 6-6-6 Read Output Measurement

6.6.3.2 Timing Margin Measurement

Caution

Use the 0 V terminal or signal ground near check terminals CH1 and CH3 for measurement, and a 200 MHz, wide band pass oscilloscope. Otherwise some measurement error may occur.

- (1) Record this worst-case data pattern "EB6DB6DB₁₆" on all records of the specific track, e.g. CE track or Cylinder 0 track.
- (2) Connect terminal CH3 on the CMZM PCB to one vertical input of the oscilloscope (DC coupled).
- (3) Connect terminal CH1 to the other vertical input channel of the oscilloscope (DC coupled).
- (4) Trigger with the positive-going edge of the CH3 signal (DTWD).
- (5) Adjust the CH1 (DLDT) signal by the potentiometer RV2 to the minimum width of the critical state, so that no errors occur for 20 seconds. See TW1 in Figure 6-6-7.
- (6) Similarly, adjust the maximum width as mentioned above. See TW2 in Figure 6-6-7.
- (7) Perform the steps (5) and (6) using each Head on the specific cylinder.
- (8) The timing margin will be specific as follows:

TTMG = TW2 (min)
$$-$$
 TW1 (max) \ge 8 ns

(9) Adjust the CH1 signal as follows:

$$T_{ADJ} = \frac{TW2 (max) + TW1 (min)}{2} = 25 \text{ ns}$$

Refer to Figure 6-6-7.

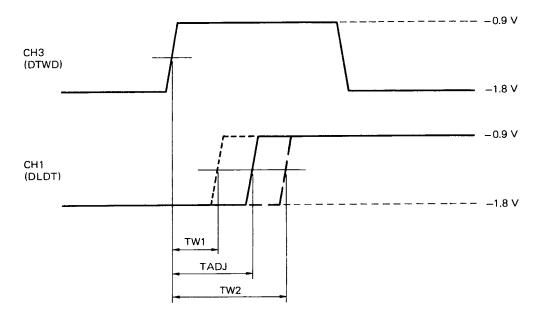


Figure 6-6-7 Timing Margin Measurement

6.6.4 Electrical Check and Adjustment

This section describes electrical checks and adjustments when an error and/or fault has occurred in the unit, or when a repair action has been performed.

Caution

Do not perform the following adjustments when the PCB is replaced.

6.6.4.1 CNAM PCB

- (1) Setting 1 (STL1) Adjustment (RV4)
 - 1. Confirm that unit has a normal status.
 - 2. Connect test point CH6 (STL1) signal one channel of the oscilloscope (DC coupled).
 - 3. Issue a repetitive RTZ command to the drive.
 - 4. Trigger the oscilloscope with the positive-going edge of the test point signal.
 - 5. Adjust potentiometer RV4 so that the following TSTL1 is 2.5 ms ± 0.1 ms (Refer to Figure 6-6-8).

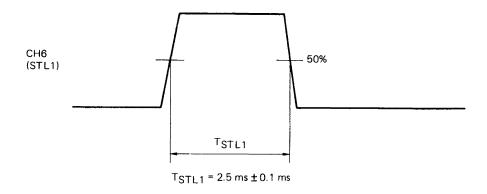


Figure 6-6-8 Settling 1 Adjustment

- (2) Reference Pulse Adjustment (RV3)
 - 1. Confirm that unit has a normal status.
 - 2. Connect test point TRM10-9 (REFP) signal to one channel of the oscilloscope (DC coupled).
 - 3. Trigger the oscilloscope with the positive-going edge of the test point signal.
 - 4. Adjust potentiometer RV3 so that the following TREF is 19 ns ± 1 ns.

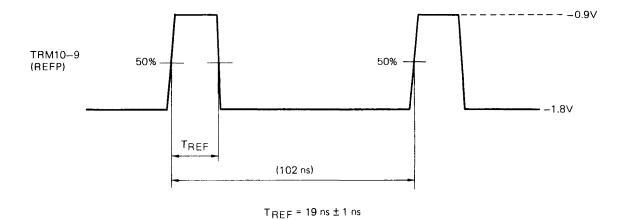


Figure 6-6-9 Reference Pulse Adjustment

- (3) VFO Free-run Frequency Adjustment (RV1)
 - 1. Turn power off.
 - 2. Remove the short plug between TRM7-14 and TRM7-03.
 - 3. Clamp the TRM7-14 signal (*FLTSQ) to 0 V.
 - 4. Turn power on and wait 40 seconds.
 - 5. Adjust potentiometer RV1 to the center position.
 - 6. Connect TRM9-13 (-2FEYB: ECL level) to a frequency counter.
 - 7. Select the proper capacitance as shown in Figure 6-6-9 so that the frequency of TRM9-13 is closest to 19.664 MHz.
 - 8. Adjust potentiometer RV1 so that the frequency of TRM9-13 is 19.664 MHz ±0.1 MHz, and connect TRM7-14 and TRM7-3 with the short-plug.

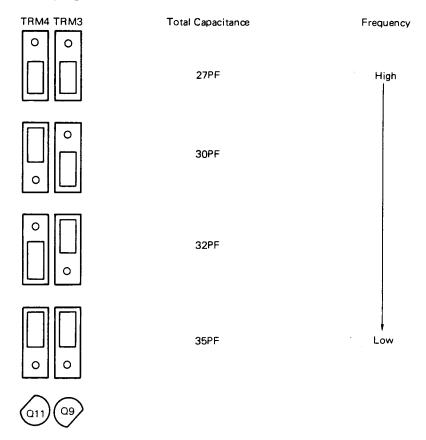


Figure 6-6-10 VFO Free-run Frequency Adjustment

(4) Timing Margin Adjustment (RV2) Refer to Section 6.6.3.2.

6.6.4.2 CMZM PCB

- (1) Write Current Adjustment (RV10)
 - 1. Confirm that unit has a normal status.
 - 2. Connect TP1 (WCA) to channel of oscilloscope and connect TP2 (WCB) to the other vertical input channel with invert mode set.
 - 3. Add the two channels (differential mode).
 - 4. Issue a write command on Cylinder 0 and Head 0.
 - 5. Adjust potentiometer RV10 so that the difference is 355 mV ± 10 mV.

(2) Read Amplifier Offset Adjustment (RV11)

1) Hard Sector Mode

When the unit is used by Hard Sector mode, this adjustment is as follows.

- 1. Confirm that unit has normal status.
- 2. Connect TP5 (AGCOT1) or TP6 (AGCOT2) to a channel of oscilloscope.
- 3. Trigger with the negative-going edge of TP3 (WG) on the CNAM PCB.
- 4. Adjust potentiometer RV1 with write enabled so that the waveform is symmetrical as shown in Figure 6-6-11.

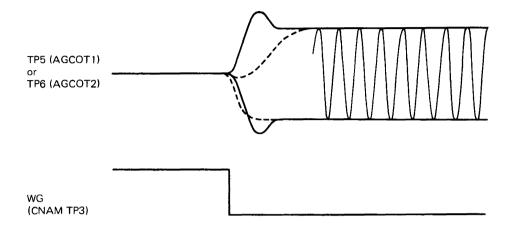


Figure 6-6-11 Read Amplifier Offset Adjustment 1

2) Soft Sector Mode

When the unit is used by Soft Sector mode, this adjustment is as follows:

- 1. Confirm that unit has normal status.
- 2. Connect TP5 or TP6 to a channel of oscilloscope.
- 3. Trigger with the negative-going edge of TP26 (*AMRD) on CNAM PCB.
- 4. Adjust potentiometer RV1 with AM-Read enabled so that the waveform is symmetrical as shown in Figure 6-6-12.

Note: Potentiometer RV1 has been adjusted in the Soft Sector Mode, before shipment from the factory.

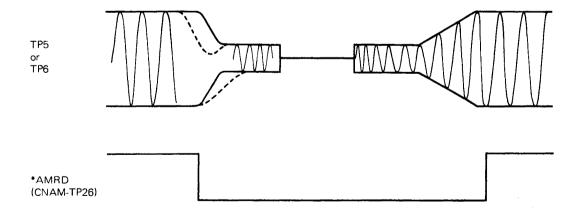
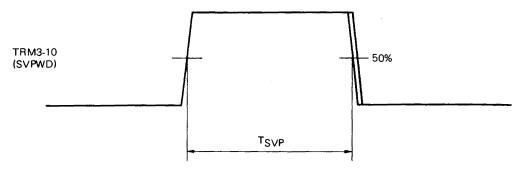


Figure 6-6-12 Read Amplifier Offset Adjustment 2

(3) Servo Pulse Window Adjustment (RV4)

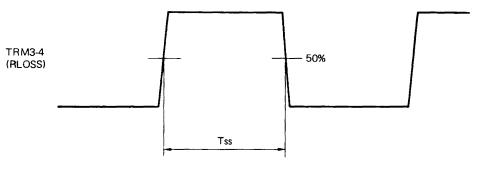
- 1. Confirm that unit has normal status.
- 2. Connect the test point TRM3-10 to an oscilloscope.
- 3. Trigger by itself at the positive-going edge.
- 4. Adjust the potentiometer RV4 so that the following TSVP is 310 ns ±10 ns.



 $T_{SVP} = 310 \text{ns} \pm 10 \text{ns}$

Figure 6-6-13 Servo Pulse Window Adjustment

- (4) PLOSS Adjustment (RV5)
 - 1. Confirm that unit has normal status.
 - 2. Connect the test point TRM3-4 (PLOSS) to an oscilloscope.
 - 3. Trigger by itself at the positive-going edge.
 - 4. Adjust potentiometer RV5 so that the following TSS is $1.5 \mu s \pm 0.1 \mu s$.



Tss = 1.5μ s $\pm 0.1\mu$ s

Figure 6-6-14 PLOSS Adjustment

- (5) PLO Free-run Frequency Adjustment (S2, S3, RV2)
 - 1. Turn the power off.
 - 2. Set S1 to the off position.
 - 3. Clamp TRM3-16 to 0V (TRM3-8).
 - 4. Turn the power on, and wait 40 seconds.
 - 5. Connect test point TRM4-7 (PLOVC) to an oscilloscope (DC coupled).
 - 6. Adjust potentiometer RV2 so that TRM4-7 signal is +2.5 V ±0.1 V.
 - 7. Connect test point TRM4-5 (BYTCLK) to a frequency counter.
 - 8. Select the proper capacitance as shown in Figure 6-6-15 so that the frequency of TRM4-5 is closest to 1.229 MHz as possible.

9. Finally adjust the potentiometer RV2 so that the frequency of TRM4-5 is 1.229 MHz ±2%.

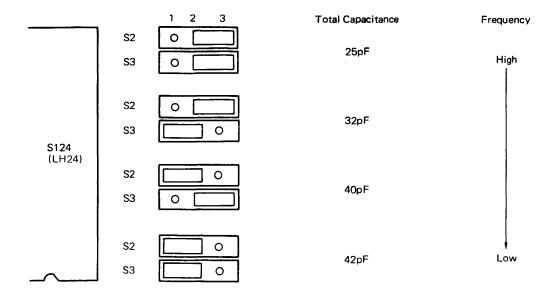


Figure 6-6-15 PLO Free-run Frequency Adjustment

- (6) Velocity Offset Adjustment (RV7)
 - 1. Confirm that unit has a normal status.
 - 2. Connect test point TRM5-2 (-VEL) to an oscilloscope.
 - 3. Adjust potentiometer RV7 so that TRM5-2 signal is 0 V ±10 mV with linear mode and without seek command.
- (7) DAC Output Adjustment (RV8)
 - 1. Confirm that unit has a normal status.
 - 2. Issue the alternate seek command between Cylinder 0 and Cylinder 192 (decimal) repeatedly.
 - 3. Connect the test point TRM6-7 (DRLM) to an oscilloscope and trigger with positive-going edge of the signal. (DC coupled)
 - 4. Connect the test point TRM5-5 (-DA) to the other channel at the oscilloscope. (DC coupled)
 - 5. Adjust a potentiometer RV8 so that V_{DA} is -6.8 V ±0.3 V as shown in Figure 6-6-16.

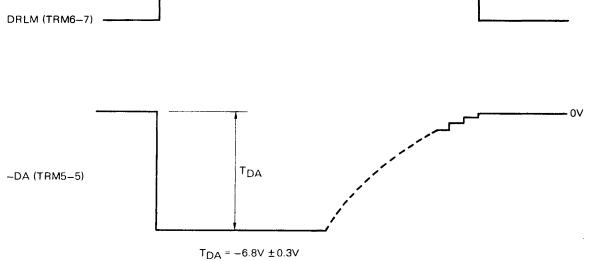


Figure 6-6-16 DAC Output Adjustment

Section 7 **Spare Parts List**

7. SPARE PARTS LIST

7.1 SPARE PARTS LIST

Refer to Table 7-1.

Table 7-1 Spare Parts List

Item	Designation	Specification
1	Controller A (CNAM) PCB Assembly	B16B-6970-0010A
2	Controller Z (CMZM) PCM Assembly	B16B-6960-0010A
3	Power Amp Z (TUZM) PCB Assembly	B16B-7640-0010A

7-1

Section 8 IC Details

8. IC DETAILS

8.1 INTRODUCTION

This section describes functions of TTL, ECL, Linear and FUJITSU Analog Master Slice IC's.

8.2 LOGIC CONVENTIONS AND SYMBOLOGY

8.2.1 TTL Logic

M231XK Micro Disk Drive uses +5V Transistor-Transistor-Logic. TTL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High Voltage = Logical "1" Low Voltage = Logical "0"

The input/output logic of TTL are defined as follows:

(A) TTL Medium Speed IC

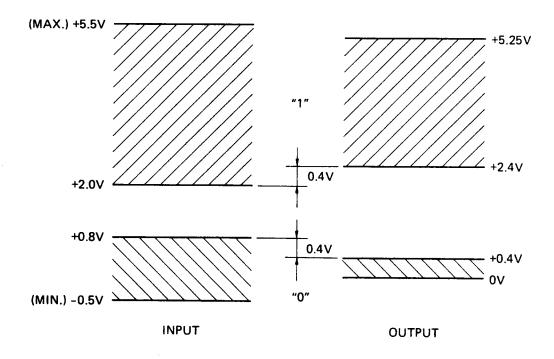


Figure 8-2-1 TTL Medium Speed IC Level

(B) TTL Super High Speed IC Level

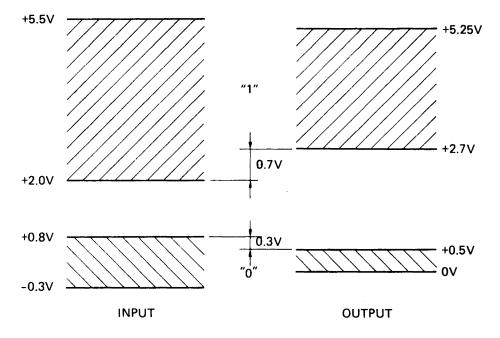


Figure 8-2-2 TTL Super High Speed IC Level

(C) TTL Medium Speed Low Power Consumption IC

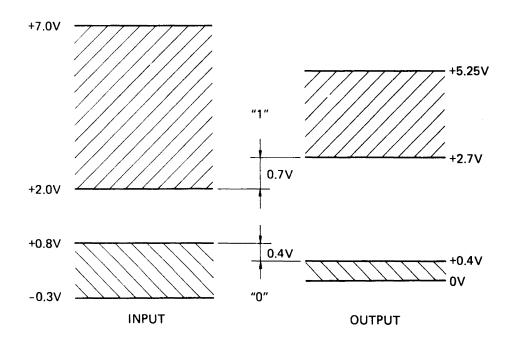


Figure 8-2-3 TTL Medium Speed Low Power Consumption IC Level

8.2.2 ECL Logic

M231XK Mirco Disk Drive uses -5.2V ECL (Emitter-Coupled-Logic). The high impedance of the logic (input to differential amplifier) coupled with the low impedance of the driving source (emitter-follower output) allows high DC fan-out.

High-speed operation and high AC fan-out are possible because all circuits are designed to operate in a 50 ohms system. Complementary outputs cause a function and its complement to appear simultaneously at the device output, without the use of external inverters. In M231X each output is terminated to resistors. ECL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

The input/output logic levels of ECL are defined as follows:

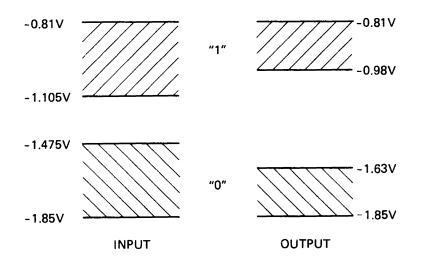
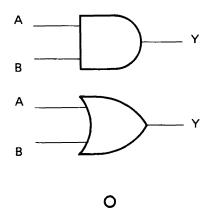


Figure 8-2-4 ECL Logic Level

8.2.3 Logic Symbology

The following conventions are provided to aid in understanding the symbology used in this manual.

1) TTL



This indicates AND gate.

$$Y = A \cdot B$$

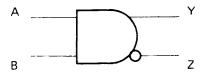
This indicates OR gate.

$$Y = A + B$$

A circle placed on any input line or on the output line indicates that logical "0" is the significant state.

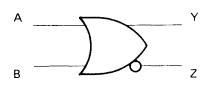
The absence of a circle, "1" is the significant state.

2) ECL



This indicates AND/NAND Gate.

$$Y = A \cdot B = \overline{Z}$$



0

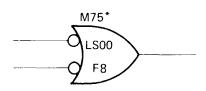
This indicates OR/NOR gate.

$$Y = A + B = \overline{Z}$$

This is equal to it of the TTL.

3) All logic symbols on each logic diagram are identified by a sequential numbering and element type code.

For example:



M75*: Sequential part number of each parts list.
LS00: Abbreviation (marking) of the element code.
F8: Physical location of element on P.C.B. assembly.

8.3 IC INTERCHANGEABILITY GUIDE

8.3.1 TTL IC Interchangeability

Table 8-3-1 TTL Interchangeability

FUJITSU		Direct		0'4	
Part Number	Code	Replacement	Functions	Q'ty	Page
MB74LS00M	LS00	SN74LS00N	Quad 2-input NAND	20	8-7
ME74LS02M	LS02	SN74LS02N	Quad 2-input NOR	5	8-7
MB74LS04M	LS04	SN74LS04N	Hex Inverter	18	8-7
MB74LS08M	LS08	SN74LS08N	Quad 2-input AND	12	8-7
MB74LS10M	LS10	SN74LS10N	Triple 3-input NAND	6	8-7
MB74LS11M	LS11	SN74LS11N	Triple 3-input AND	4	8-8
MB74LS14M	LS14	SN74LS14N	Hex Schmitt-Triggered Inverter	1	8-8
MB74LS20M	LS20	SN74LS20N	Dual 4-input NAND	1	8-8
MB74LS27M	LS27	SN74LS27N	Triple 3-input NOR	2	8-8
MB74LS30M	LS30	SN74LS30N	Single 8-input NAND	1	8-8
MB74LS32M	LS32	SN74LS32N	Quad 2-input OR	6	8-9

Table 8-3-1 TTL Interchangeability (Continued)

FUJITSU		Direct	Functions	Q'ty	Page	
Part Number	Code	Replacement	, direttons			
MB74LS37M	LS37	SN74LS37N	Quad 2-input NAND Buffer	5	8-9	
MB74LS42M	LS42	SN74LS42N	4-line-to-10-line Decoder	3	8-16	
MB74LS51M	LS51	SN74LS51N	Dual 2-wide 2-input AND-OR-INVERT	2	8-9	
MB74LS74AM	LS74	SN74LS74AN	Dual D-type Positive-Edge-Triggered Flip-Flop	12	8-11	
MB74LS85M	L\$85	SN74LS85N	4-bit Magnitude Comparator	4	8-23	
MB74LS86M	LS86	SN74LS86N	Quad 2-input EOR	3	8-9	
MB74LS107M	LS107	HD74LS107P	Dual J-K Master/Slave Flip-Flop	6	8-12	
-	LS123	SN74LS123N	Dual Retriggerable Monostable Multivibrator with Clear	2	8-12	
MB74LS139M	LS139	SN74LS139N	Dual Decoder 1		8-17	
MB74LS153M	LS153	SN74LS153N	Dual 4-line-to-1-line Data Selector/Multiplexer	3	8-25	
MB74LS161AM	LS161	SN74LS161AN	4-bit Binary Counter	20	8-18	
MB74LS164M	LS164	SN74LS164N	8-bit Shift Register	3	8-22	
MB74LS175M	LS175	SN74LS175N	Quad D-type Flip-Flop	7	8-14	
MB74LS191M	LS191	SN74LS191N	4-bit Binary Up/Down Counter	3	8-20	
-	LS221	SN74LS221N	Dual Monostable Multivibrator with Clear	3	8-13	
_	LS279	SN74LS279N	Quad S-R Latch	5	8-11	
MB74LS283M	LS283	SN74LS283N	4-bit Full Adder	4	8-24	
MB434M	434	SN75451BP	Dual 2-input AND Buffer with Open-collector	7	8-9	
MB436M	436	SN75453BP	Dual 2-input OR Buffer with Open-collector	1	8-10	
-	LX16	SN75452BP	Dual 2-input NAND Buffer with Open-collector	2	8-10	
-	LX26	SN74175N	Quad D-type Flip-Flop	1	8-14	
	LX31	SN74148N	8-to-3 Priority Encoder	2	8-26	
-	LX32	SN7406N	Hex Inverter with Open-collector	2	8-10	
-	LX33	SN7407N	Hex Buffer with Open-collector	2	8-10	
MB74S00N	LH01	SN74S00N	Quad 2-input NAND	1	8-7	
MB74S04N	LH04	SN74S04N	Hex Inverter	3	8-7	
_	LH10	SN74S112N	Dual J-K Negative-Edge-Triggered Flip-Flop with Preset and Clear	1	8-11	
_	LH24	SN74S124N	Dual VCO	1	8-27	

Note 1) Direct Replacement is a device of Texas Instruments Inc. except LS107 (HD74LS107P).

²⁾ Direct Replacement of LS107 is a device of Hitachi Ltd.

8.3.2 ECL IC Interchangeability

Table 8-3-2 ECL Interchangeability

FUJIT	SU	Direct	Functions	Q'ty	Page
Part Number	Code	Replacement	runctions	Q ty	raye
MB10102C	102	MC10102L	Quadruple 2-input NOR	8	8-28
MB10105C	105	MC10105L	MC10105L Triple 2-3-2 input OR/NOR		8-28
MB10106C	106	MC10106L	Triple 4-3-3 input NOR		8-28
MB10115C	115	MC10115L	Quad Receiver	1	8-29
MB10116C	116	MC10116L	Triple Receiver	1	8-29
MB10121C	121	MC10121L	4-wide OR-AND/ OR-AND-INVERT	1	8-29
MB10124C	124	MC10124L	Quadruple TTL to ECL Translator	4	8-30
MB10125C	125	MC10125L	Quadruple ECL to TTL Translator	1	8-30
MB10131C	131	MC10131L	Dual D-type Master-Slave Flip-Flop	9	8-31
MB10162C	162	MC10162L	Binary 1-to-8 Decoder	2	8-32

Note: Direct replacement is a device of MOTOROLA Semiconductor. Product Inc.

8.3.3 Linear IC Interchangeability

Table 8-3-3 Linear IC Interchangeability

FUJIT	SU	Direct	Functions	01	
Part Number	Code	Replacement	Functions	Q'ty	Page
MB3607M	A1458	μPC251C (NEC)	Dual 741-type Operational Amplifier	16	8-33
MB4002M	A4002		High Speed Voltage Comparator	1	8-33
	A311	μPC271C (NEC)	311-type Voltage Comparator	19	8-34
	A1590	MC1590G (MOTOROLA)	AGC Amplifier	1	8-35
	A399	μPC177C (NEC)	339-type Voltage Comparator	1	8-35
	A610	μPC610D (NEC)	8-bit D/A Converter	1	8-36
	A201	DG201BK (Siliconix)	Quad SPST Analog Switch	6	8-37
	A7812	μPC14312H (NEC)	7812-type +12V Regulator	1	8-37
	A7952	μPC16352H (NEC)	7952-type –5.2V Regulator	1	8-37
		MC3450L (MOTOROLA)	Quad Line Receiver	5	8-38
	75108A	SN75108AN (TI)	Dual Line Receiver with Open-Collector	2	8-38
	75110	SN75110AN (TI)	Dual Line Driver	8	8-38

8.3.4 FUJITSU Proprietary IC

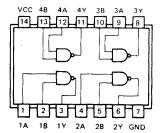
Table 8-3-4 FUJITSU Proprietary IC List

FUJITSU		- 01	-		_					
Part Number	Code	Classification	Functions	Q'ty	Page					
MB4303C	A4303	Analog Master-Slice	AGC Amplifier	1	8-39					
MB4311C	A4311	Analog Master-Slice Peak Detector 1	ster-Slice Peak Detector		Peak Detector 1	1	8-39			
MB4316C	A4316	Analog Master-Slice	Read/Write Bus Switch	1	8-40					
MB4319C	A4319	Analog Master-Slice	Peak Hold	1	8-40					
MB4320C A4320	MB4320C	A4320	Analog Master-Slice Pulse Shaper						1	8-41
MB14601M	14601	Bipolar 200-gate	Linear Motor Control	1	8-42					
	DV18	Hybrid IC	Clock Driver	1	8-41					

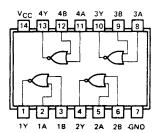
8.4 IC DETAIL

8.4.1 TTL Detail

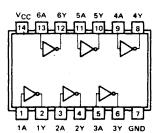
1) MB74S00M (SN74S00N)
MB74LS00M (SN74LS00N)
Quadruple 2-Input
Positive NAND Gates
Positive Logic $Y = \overline{A \cdot B}$



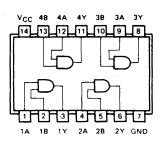
2) MB74LS02M (SN74LS02N)
Quadruple 2-Input
Positive NOR Gates
Positive Logic $Y = \overline{A + B}$



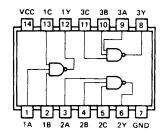
3) MB74LS04M (SN74LS04N)
MB74 S04M (SN74S04N)
Hex Inverters
Positive Logic
Y = A



4) MB74LS08M (SN74LS08N)
Quadruple 2-Input
Positive AND Gates
Positive Logic
Y = A · B



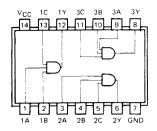
5) MB74LS10M (SN74LS10N)
Triple 3-Input
Positive NAND Gates
Positive Logic
Y = A·B·C



6) MB74LS11M (SN74LS11)

Triple 3-Input
Positive AND Gates

 $Y = A \cdot B \cdot C$

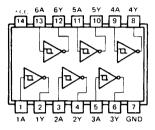


7) MB74LS14M

Hex Schmitt-Trigger Inverters

Positive Logic

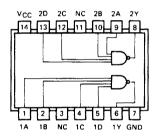
 $Y = \overline{A}$



8) MB74LS20M (SN74LS20N)

Dual 4-Input Positive NAND Gates Positive Logic

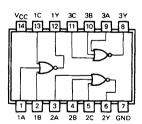
 $Y = \overline{A \cdot B \cdot C \cdot D}$



9) MB74LS27M

Triple 3-Input NOR Gates Positive Logic

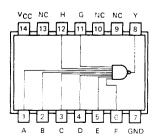
 $Y = \overline{A + B + C}$



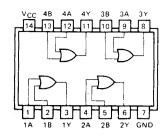
10) MB74LS30M (SN74LS30M)

8-Input Positive NAND Gates Positive Logic

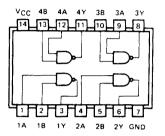
 $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$



11) MB74LS32M (SN74LS32N)
Quadruple 2-Input
Positive OR Gates
Positive Logic
Y = A + B



12) MB74LS37M (SN74LS37N)
Quadruple 2-Input
Positive NAND Buffers
Positive Logic
Y = A·B

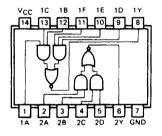


13) MB74LS51M (SN74LS51N)

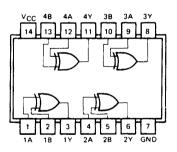
Dual 2-Wide 2-Input

AND-OR-INVERT Gates

Positive Logic



14) MB74LS86M (SN74LS86N)
Quadruple 2-Input
Exclusive OR Gates
Positive Logic Y = A + B = AB + AB



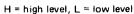
15) MB434M (SN75451B)

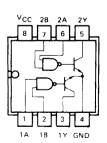
Dual Peripheral Positive AND Driver

Positive Logic

$$Y = A \cdot B$$
FUNCTION TABLE

Α	В	Y
L	L	L (on state)
L	Н	L (on state)
Н	L	L (on state)
Н	Н	H (off state)



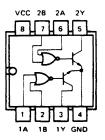


16) MB436M (SN75453B)

Dual Peripheral Positive OR Driver Positive Logic

Α	В	Υ
L	L	L (on state)
L	Н	H (off state)
н	L	H (off state)
н	Н	H (off state)

H = high level, L = low level



17) SN75452B

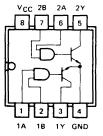
Dual Peripheral Positive NAND Driver Positive Logic

$$Y = \overline{A \cdot B}$$

FUNCTION TABLE

Α	В	Υ	
L	L	H (off state)	
L	Н	H (off state)	
н	L	H (off state)	
н	Н	L (on state)	

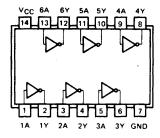
H = high level, L = low level



18) SN7406N

Hex Inverter with Open-collector Positive Logic

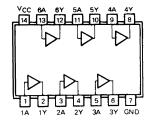
$$Y = \overline{A}$$



19) SN7407N

Hex Buffer with Open-Collector Positive Logic

$$Y = A$$



20) MB74LS279M (SN74 LS279N)

Quadruple S-R Latches

FUNCTION TABLE

INPI	JTS R	OUTPUT Q
HLHL	HHLL	91 - I



L = low level

 Q_0 = the level of Q before the indicated input conditions were established.

*This output level is pseudo stable; that is, it may not persist when the \$\overline{S}\$ and \$\overline{R}\$ inputs return to their inactive (high) level.

† For latches with double \$\overline{S}\$ inputs:

H = both \$\overline{S}\$ inputs high

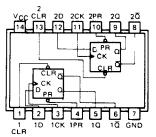
L = one or both \overline{S} inputs low

21) MB74LS74M (SN74LS74N)

Dual D Type Positive Edge Triggered Flip-Flop with Preset and Clear

FUNCTION TABLE

INPUTS					PUTS
PRESET	CLEAR	CLOCK	D	a	ā
JIJIII	# L L # # #	X X † †	XXXHLX	T H T L Q	OH-HHO



H = high level (steady state), L = low level (steady state), X = irrelevant

= high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

 \uparrow = transition from low to high level, \downarrow = transition from high to low level

Q₀ = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

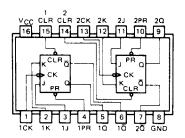
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

22) SN74S112N

Dual J-K Negative Edge Triggered Flip-Flop with Preset and Clear

FUNCTION TABLE

	INPUTS					
PRESET	CLEAR	CLOCK	J	Κ	a	₫
L	Н	x	Х	Х	Н	Г
Н	L	Х	Х	X	L	н
L	L	X	Х	Х	Н*	н*
Н	Н	↓	L	L	00	₫o
Н	Н	↓	Н	L	H	Ľ
) H	Н	↓	Н	Н	TOG	GLE
Н	Н	н	X	Х	σ_0	₫o



H = high level (steady state), L = low level (steady state), X = irrelevant

 \downarrow = transition from high to low level

 Q_0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock

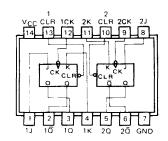
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

23) MB74LS107M (SN74LS107N)

Dual J-k Mater Slave Flip-Flop with clear

FUNCTION TABLE

10											
	OUTPUTS										
CLEAR	CLOCK	J	K	Q	ā						
L	х	Х	X	L	Н						
H		L	L	σ0	ΩO						
н		Н	L	н	L						
н		L	Н	L	н						
Н		Н	Н	TOG	GLE						



H = high level (steady state), L = low level (steady state), X = irrelevant

 Q_0 = the level of Q before the indicated input conditions were established.

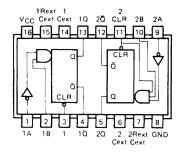
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

24) SN74LS123N

Dual Retriggerable Monostable Multivibrator with Clear

FUNCTION TABLE

INPL	INPUTS								
CLEAR	А	В	a	ā					
L	х	Х	L	Н					
×	Н	X	L	н					
×	×	L	L	Н					
н	L	1	<u></u>	7					
Н	↓	Н	_√_	7					
↑	L	н		7					



This monolithic TTL retriggerable monostable multivibrator features d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provides overriding direct clear inputs. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse terminated, the output pulses may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. The output pulse is primarily a function of the external capacitor and resistor.

For Cext > 1000pF, the output pulse width (tw) is defined as:

tw: ns

tw = 0.32RtCext $(1 + \frac{0.7}{Rt})$ Rt : kohms

Cext : pF

^{↓ =} transition from high to low level

⁼ high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

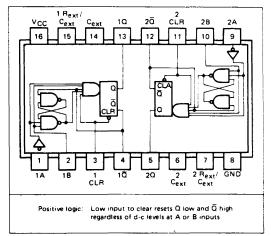
^{*} This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

25) SN74LS221N **Dual Monostable Multivibrator** with Schmitt-Trigger Input

The SN74LS221N are monolithic dual multivibrators with performance characteristics virtually identical to those of the SN74121N. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to Vcc noise of typically 1.5 volts is also provided by internal latching circuitry.

(TOP VIEW)



FUNCTION TABLE (EACH MONOSTABLE)

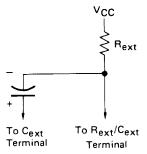
	INPUTS	OUTPUTS								
CLEAR	Α	В	Q	ā						
L	X	Х	L	Н						
×	Н	×	L	н						
×	×	L	L	н						
н	L	0	_√_	7						
н	↓	н		7.						
1	L	н	工	7						
	Also see description and switching									

characteristics

The output pulse width (tw) is defined as:

tw = 0.7RextCext

tw; ns, rext: kohms, Cext: pf



TIMING COMPONENT CONNECTIONS

26) SN74175N MB74LS175M (SN74LS175N) Quadruple D-Type Flip-Flop

MB74LS174M (SN74LS174N) Hex D-Type Flip-Flop

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175' and LS175 feature complementary outputs from each flip-flops.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	оит	PUTS	
CLEAR	CLOCK	D	a	Q٢
L	×	×	L	Н
н	t	H	н	L
н	t	L	L	н
Н	L	X	σ0	\bar{a}_0

H = high level (steady state)

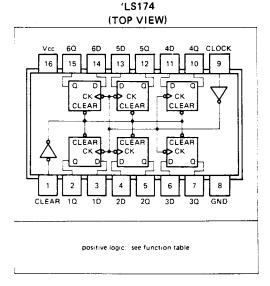
L = low level (steady state)

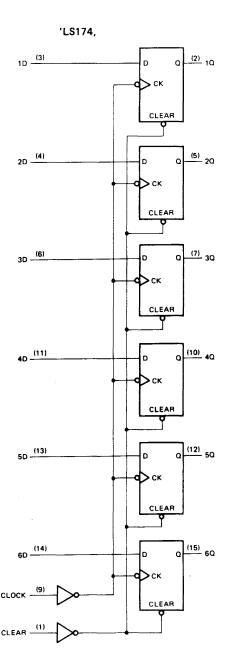
X = irrelevant

t = transition from low to high level

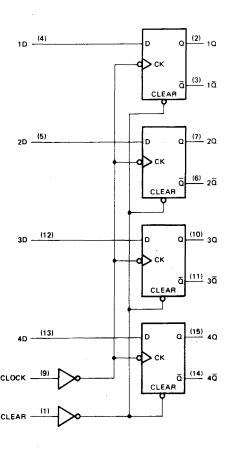
 Q_0 = the level of Q before the indicated steady-state input conditions were established.

† = '175, 'LS175, only





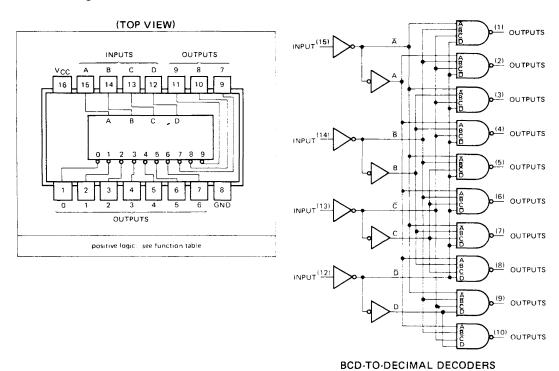
'175, 'LS175,



... dynamic input activated by transition from a high level to a low level.

27) MB-74LS42M BCD-to-Decimal Decoder

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.



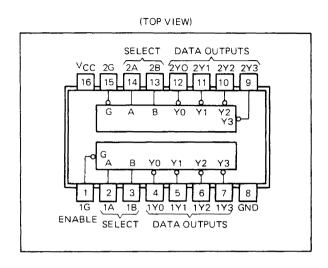
FUNCTION TABLE

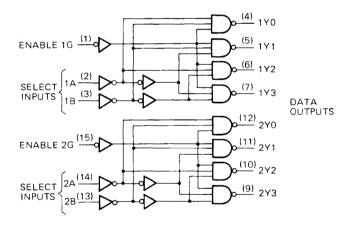
	вс	DI	NPI	IJΤ			DE	CIN	1AL	. 01	JTF	TU		
No.	D	С	В	Α	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
1	L	L	L	Н	н	L	Н	Н	Н	Н	Н	Н	Н	н
2	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	н
3	L	L	Н	Н	н	Н	Н	L	Н	Н	Н	Н	Н	н
4	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	н
5	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
6	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
7	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	н
8	Н	L	Ľ	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
9	Н	L	L	Н	н	Н	Н	Н	Н	Н	Н	Н	Н	L
	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Ξ
	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
INVALID	Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	н
Ιź	Н	Н	Н	L	н	Н	Н	Н	Н	Н	Н	Н	Н	Н
	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	н

H = high level, L = low level

28) MB74LS139M Dual 2-Line-to-4-Line Decoder

The LS139 comprises to individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.





(EACH DECODER/DEMULTIPLEXER) FUNCTION TABLE

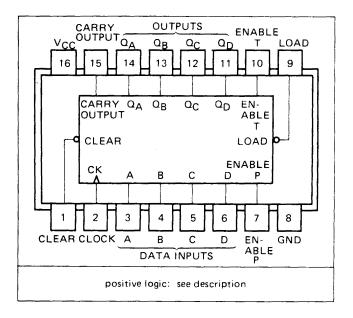
INPL	JTS	OUTDUTE					
ENABLE	SEL	ECT	OUTPUTS .				
G	В	Α	Y0	Y1	Y2	Y3	
н	х	Х	н	Н	Н	н	
L	L	L	L	Н	Н	Н	
L	L	Н	н	L	Н	н	
L	Н	L	н	Н	L	Н	
L	Н	н	н	Н	н	L	

H = high level, L = low level, X = irrelevant

Synchronous 4-bit Counter with Direct Clear

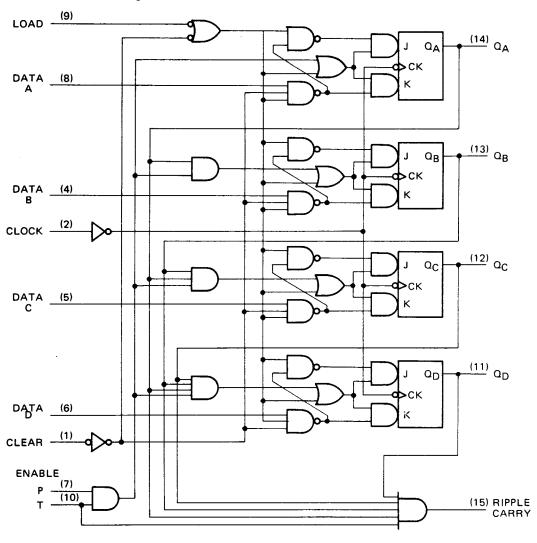
This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting schemes. Synchronous operation is provided by having all flip-flop clocked simultaneously so that the outputs change coincident with each other when so instructed by the countenable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K masterslave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function for the SN74161N is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).



8-18 B03P-4590-0103A...A

Functional block diagrams

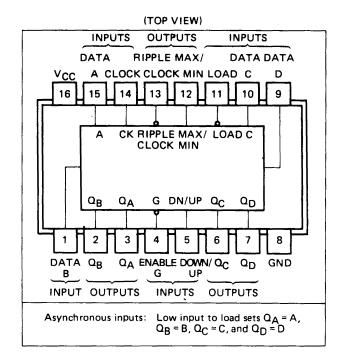


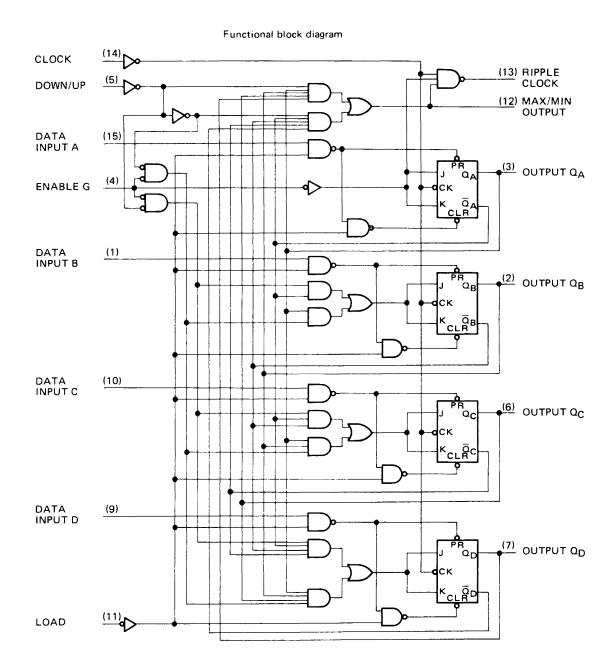
30) MB74LS191M Synchronous UP/DOWN Counters with DOWN/UP Mode Control

The LS191 is synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The LS191 is 4-bit binary counters. Synchronous operation is provided by having all flip-flop clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flop are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the present inputs.

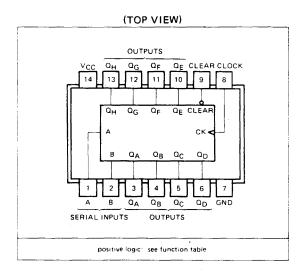




31) MB74LS164M

8-Bit parallel-Out Serial Shift Registers

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.



FUNCTION TABLE

	INPUTS	OUTPUTS				
CLEAR	CLOCK	Α	В	QA	Ag .	QH
L	Х	х	Х	L	L	L
Н	L	X	X	QAO	Q _{BO}	a_{H0}
н	1	H	Н	Н	QAn	Q_{Gn}
Н	↑	L	X	L	Q_{An}	Q_{Gn}
Н	1	X	L	L	Q_{An}	α_{Gn}

H = high level (steady state), L = low level (steady state)

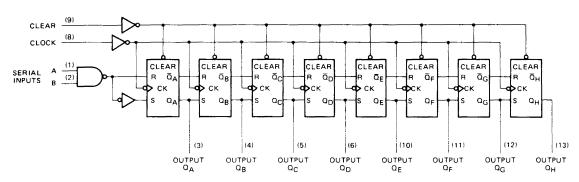
X = irrelevant (any input, including transitions)

1 = transition from low to high level.

 Ω_{A0} , Ω_{B0} , Ω_{H0} = the level of Ω_A , Ω_B , or Ω_H , respectively, before the indicated steady-state input conditions were established.

 Q_{An} , Q_{Gn} = the level of Q_{Aor} Q_{G} before the most-recent \uparrow transition of the clock; indicates a one-bit shift.

Functional block diagram



_________. . . . dynamic input activated by transition from a high level to low level

32) MB74LS85M

4-bit Magnitude Comparators

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits.

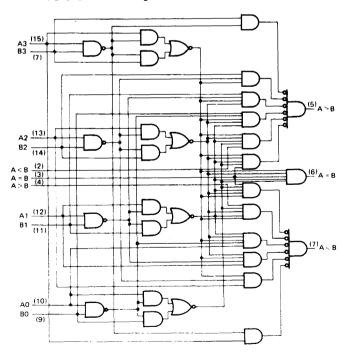
FUNCTION TABLES

	COMP/ INP	ARING UTS	_	SCAD!	-	OUTPUTS			
A3, B3	A2, B2	A2, B2 A1, B1 A0, 80		A > B	A < B	Ą = B	A>B	A < B	A = B
A3 > B3	×	×	×	х	×	×	н	L	L
A3 < B3	×	×	×	×	×	×	L	н	L
A3 = B3	A2 > B2	x	×	×	х	×	Н	L	L
A3 = B3	A2 < B2	×	x	×	X	×	L	н	L
A3 = B2	A2 = B2	A1 > B1	×	×	х	X	н	L	L
A3 = B3	A2 = B2	A1 < B1	×	x	X	X	L	н	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	×	×	X	н	L	L
A3 = B3	A2 = 82	A1 = B1	A0 < B0	×	X	X	L	н	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	н	L	L	н	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	н	L
A3 ≃ B3	A2 = B2	A1 = B1	A0 = B0	L	L	Н	L	L	н
A3 = B3	A2 = B2	A1 = B1	A0 = B0	х	×	Н	L	L	н
A3 = B3	A2 = B2	A1 = B1	A0 = B0	н	н	L	L	L	L
A3 = B3	A2 ≈ B2	A1 = B1	A0 = B0	L	Ł	L	н	н	L

JOR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW) INPUTS OUTPUTS А3 A>B A<B во 16 15 13 12 11 10 9 14 A=R A>R A<B A=B INPUTS INPUTS Positive logic: See function tables

H = high level, L = low level, X = irrelevant

Functional block diagrams



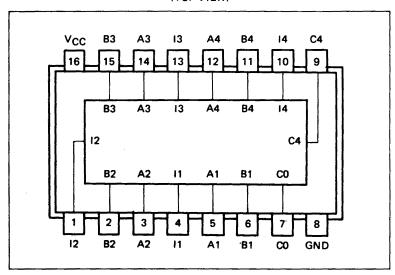
33) MB74LS283M

4-Bit Binary Full Adders with Fast Carry

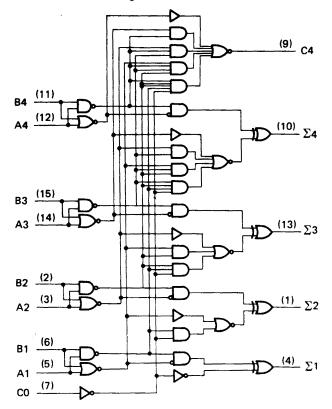
These improved 4-Bit full adders/subtractors feature full look-ahead across four bits to generate the carry term in typically 10 nanoseconds. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

These full adders are designed so that levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

(TOP VIEW)



Functional block diagram



34) MB74LS153M (SN74LS153N) Dual 4-Line-to-Line Data Selectors/Multiplexers

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-inverter gates. Separate strobe inputs are provided for each of the two four-line sections.

(TOP VIEW)

STROBE A

VCC 2G SELECT

16 15 14 13 12 11 10 9

2C3 2C2 2C1 2C0 2V

2G 8 B A Ā

1C3 1C2 1C1 1C0 1V

Positive logic: See function table

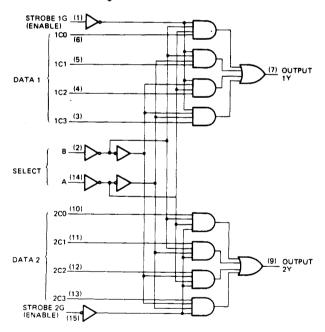
FUNCTION TABLE

	ECT UTS		DATA	STROBE	ООТРОТ		
В	A	CO	C1	C2	С3	G	V
х	Х	х	X	х	х	н	L
L	L	L	×	×	x	L	L
L	L	н	×	×	X	L	н
L	н	×	L	×	X	L	L
L	н	×	н	×	х	L	н
н	L	×	×	L	×	L	L
н	L	×	×	н	X	L	н
Н	н	×	×	×	Ł	L	L

Select inputs A and B are common to both sections.

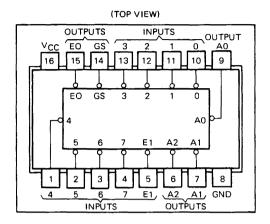
H = high level, L = low level, X = irrelevant

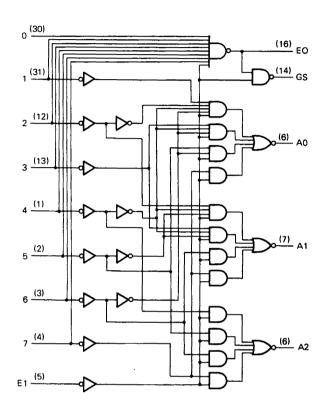
Functional block diagram



35) SN74148N 8-Line-to-3-Line Priority Encoder

The 148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable input EO) is provided to allow octal expansion without external circuitry.





FUNCTION TABLE

	INPUTS										JTPU	TS	
ΕI	0	1	2	3	4	5	6	7	A2	Α1	A0	GS	EO
Н	х	Х	х	х	Х	х	X	Х	Н	Н	Н	Н	н
L	н	н	Н	н	Н	н	н	Н	н	н	н	н	L
L	×	х	х	×	X	X	X	L	L	L	L	L	н
L	×	X	х	×	×	X	L	Н	L	L	н	L	Н
L	×	X	×	X	×	L	Н	Н	L	н	L	L	Н
L	×	×	X	X	L	Н	Н	Н	L	Н	Н	L	Н
L	×	X	х	L	Н	Н	Н	н	н	L	L	L	н
L	×	X	L	н	Н	Н	Н	Н	н	L	H	L	Н
L	x	L	Н	Н	Н	н	Н	Н	н	н	L	L	Н
L	L	н	н	н	H	н	н	Н	Н	н	н	L	н

36) SN74S124N

Dual Voltage Controlled Oscillators

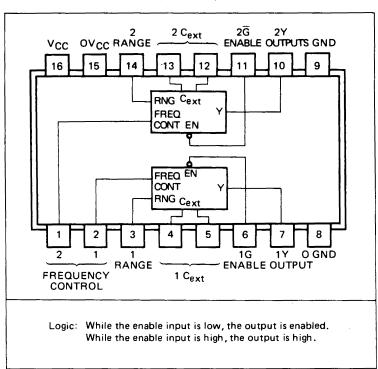
The 'S124 feature two independent voltage-controlled oscillators (VCO) in a single monolithic chip. The output frequency of each VCO is established by a single external component, either a capacitor or a crystal, in combination with two voltage-senstive inputs, one for frequency range and one for frequency control. These inputs can be used to vary the output frequency as shown under typical characteristics for the 'S124. These highly stable oscillators can be set to operate at any frequency typically between 0.12 hertz and 85 megahertz. The output frequency can be approximated as follows:

$$f_0 = \frac{5 \times 10^{-4}}{C_{\text{ext}}}$$

where: fo = output frequency in hertz

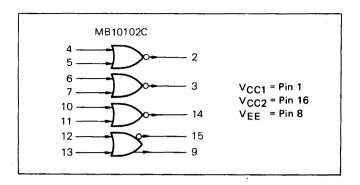
Cext = external capacitance in farads.

(TOP VIEW)

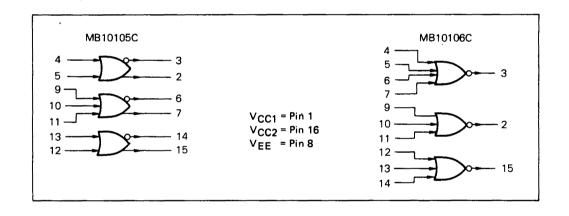


8.4.2 ECL Detail

1) MB10102C (MC10102L) Quadruple 2-input NOR

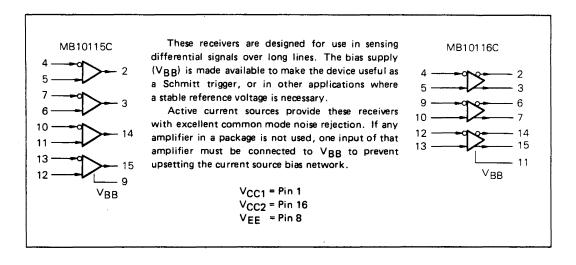


- 2) MB10105C (MC10105L) Triple 2-3-2-input OR/NOR
- 3) MC10106C (MC10106L) Triple 4-3-3-input NOR

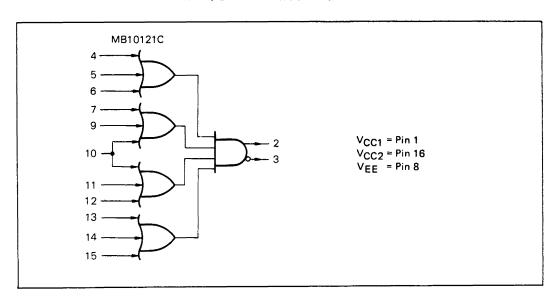


4) MB10115C (MC10115L) Quad Receiver

5) MB10116C (MC10116L) Triple Receiver



6) MB10121C (MC10121L) 4-wide OR-AND/OR-AND INVERT



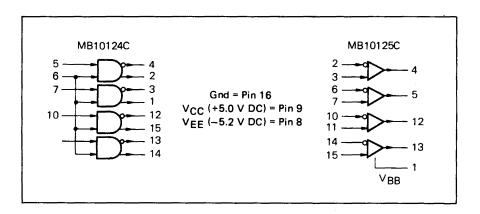
- 7) MB10124C (MC10124L)

 Quad TTL to ECL Translator
- 8) MB10125C (MC10125L)

 Quad ECL to TTL Translator

The 10124 and 10125 are quad translators for interfacing data and control signals between a high speed ECL section and low speed saturated logic sections of digital equipment. The 10124 has standard TTL inputs and standard ECL, complementary, open-emitter outputs. The 10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. These devices are useful in computers, instrumentation, peripheral controllers, test equipment and digital communication systems.

Power supply requirements are ground, +5 V DC and -5.2 V DC. Propagation delay of the 10124 is typically 5 ns. The outputs are identical to those of a standard ECL gate. An advantage of this gate is that the translation can be done in the TTL equipment and then the information can be transmitted, via balanced twisted pair, to the ECL equipment. This isolates the ECL logic from the noisy TTL environment. The 10125 has a typical propagation delay of 5 ns with a fanout of 10 TTL loads. The high speed of both these functions makes them ideal for high speed instrumentation systems and digital communication systems.

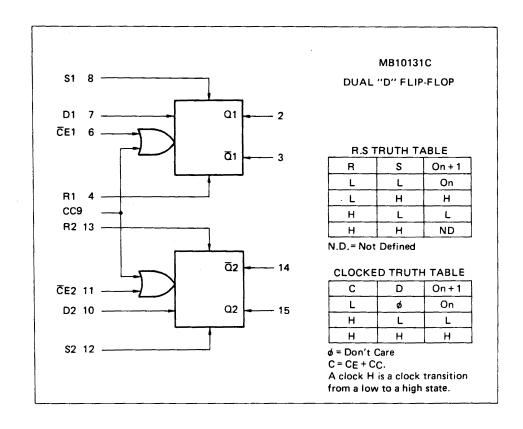


9) MB10131C (MC10131L) Dual D-Type Flip-Flop

Dual flip-flops are standard ECL with 10,000 storage and counting functions. The inputs incorporate high-impedance pulldown resistors. Emitter-follower outputs are left open for maximum flexibility and minimum power dissipation. These functions are very useful for control and storage in high-speed digital communication systems, instrumentation and test equipment, high speed central processors, high speed peripheral controllers and minicomputers.

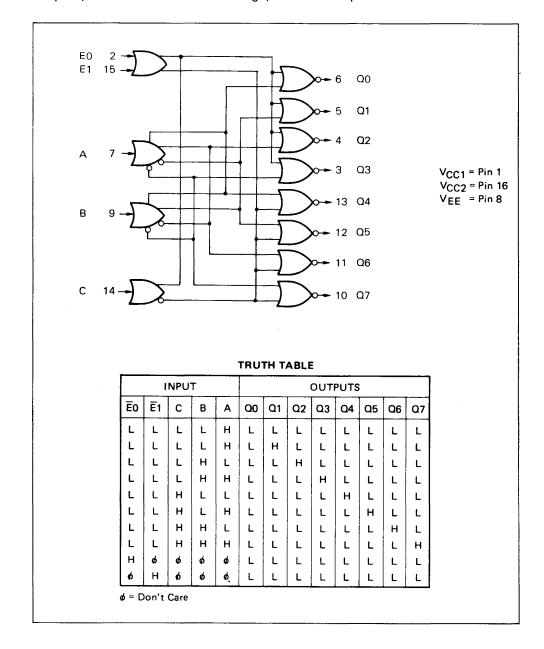
The 10131 is a high-speed dual D master slave flip-flop with asynchronous set and reset inputs, true and complement outputs.

Set and reset inputs override the clock for asynchronous operation of the 10131.



10) MB10162C (MC10162L) Binary 1-to-8 Decoder

The 10162 converts three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all output low.

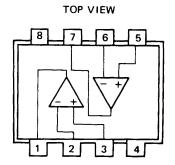


8.4.3 Linear IC Detail

1) MB3607M (MC1458C)

Dual Operational Amplifier

The MB3607M is designed for use as a summing amplifier integrator, or amplifier with operating characteristics as a function of the external feedback components.

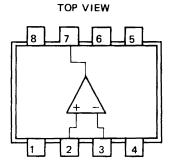


1: OUTPUT 1 2: INPUT 1 (-) 3: INPUT 1 (+) 4: V-5: INPUT 2 (+) 6: INPUT 2 (-) 7: OUTPUT 2 8: V+

2) MB4002M

High Speed Differential Comparator

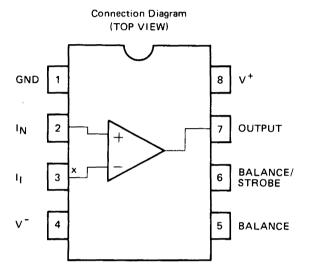
The MB4002M is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

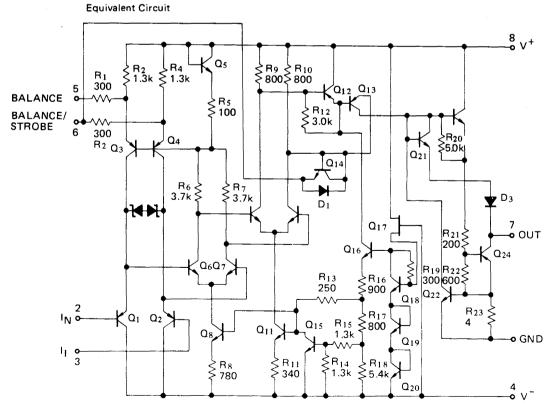


1: GND 2: INPUT (+) 3: INPUT (-) 4: V⁻ 5: NC 6: NC 7: OUTPUT 8: V⁺

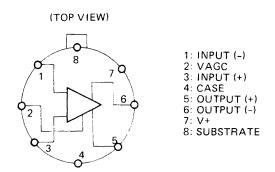
3) μ pc271C Voltage Comparator

This is a single high-speed voltage comparator. This device is designed to operate from a wide range of power supply voltage, including ± 15V supplies for operational amplifiers and +5 V supplies for logic systems. The output level is compatible with most DTL, TTL, and MOS circuits. This comparator is capable of driving Lamps or relays and switching voltage up to 50V at 50mA. All inputs and outputs can be isolated from system ground. The output can drive loads referenced to ground, Vcc+, Vcc-. Offset balancing and strobe capability are available and the output can be wire-OR connected. If the strobe input is low, the output will be in the off state regardless of the differential input.

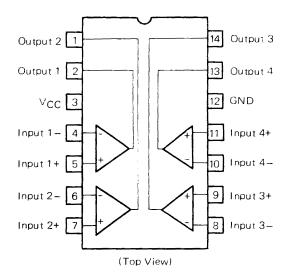




4) MC1590G AGC Amplifier



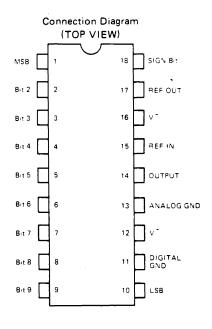
5) μ PC 177C 339-type Voltage Comparator

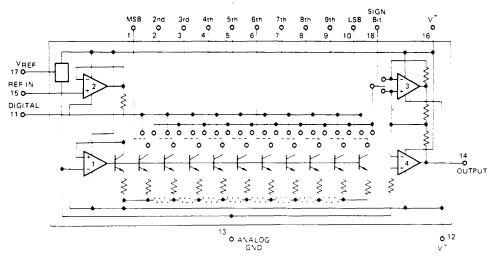


8-35

6) μPC610D 10 bit D/A Convertor

The μ PC610D is a complete 10bit plus sign D/A convertor. All elements of a complete sign/magnitude DAC are included-precision voltage reference, current steering logic, current sources, R-2R resister network, logic controlled polarity switch, and high-speed, internally compensated output of amp. The wide power supply range, low power consumption, choice of full-scale output voltages and sign/magnitude coding assure utility in a wide range of applications.

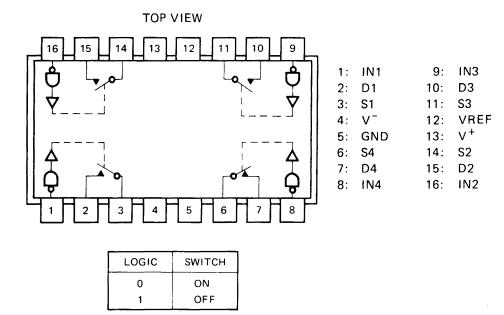




7) DG201BK

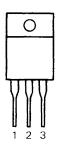
Quad Mono lithic SPST CMOS Analog Switch

The DG201 is a 4-channel single pole signal throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0V to 0.8V) the switch will be ON, and a logic "1" (2.4V to 15V) will turn the switch OFF. Switch action is break-before-make.



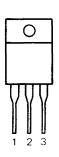
8) μ PC14312H 7812-type +12VDC Regulator

Pin 1 INPUT 2 GND 3 OUTPUT



9) μPC16352H 7905.2-type –5.2VDC Regulator

> Pin 1 GND 2 INPUT 3 OUTPUT



10) MC3450L

Quad Line Receivers

TRUTH TABLE

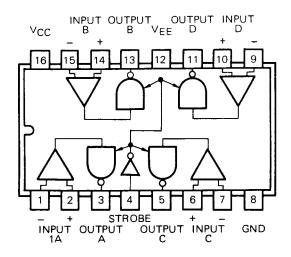
INPUT	STROBE	OUTPUT
	L	н
V _{ID} ≥ +24mV	Н	Z
-25mV < Vin	L	-
-25mV < V _{ID} < +24 mV	Н	Z
	L	L
V _{ID} ≤ +24 mV	Н	Z

L: Low Logic Stage

H: High Logic State

Z: Third (High Impedance) State

1: Indeterminate State

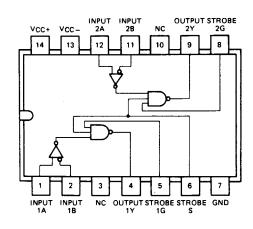


11) SN75108AN

Dual Line Receivers with Open-collector

TRUTH TABLE

DIFFERENTIAL	STR	OBES	ОИТРИТ
INPUTS A-B	G	S	Y
V _{ID} ≥ 25mV	L or H	L or H	н
	L or H	L	н
-25mV < V _{ID} < 25mV	L	L or H	н
	н	Н	INDETERMINATE
	L or H	L	н
V _{ID} ≤ -25mV	L	L or H	н
	Н	Н	L

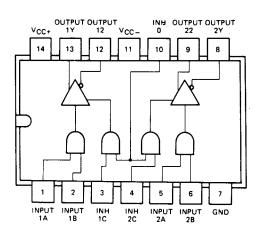


12) SN75110AN Dual Line Drivers

TRUTH TABLE

LOGIC	INPUTS		SITOR UTS	оит	PUTS
Α	В	С	D	Υ	Z
LorH	L or H	L	L or H	Н	Н
LorH	L or H	L or H	L	Н	н
L	L or H	Н	н	L	Н
L or H	L	н	Н	L	Н
Н	н	H	Н	Н	L

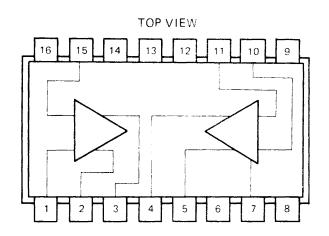
Low output represents the on state. High output represents the off state.



8.4.4 FUJITSU Proprietary IC Detail

1) MB4303C AGC Amplifier

The MB4303C is a Automatic-Gain-Control Amplifier with Differential Inputs and Outputs. It contains another Differential Amplifier.



- 2) MB4311C Peak Detector
- TOP VIEW

 16 15 14 13 12 11 10 9

 AMP

 CMP

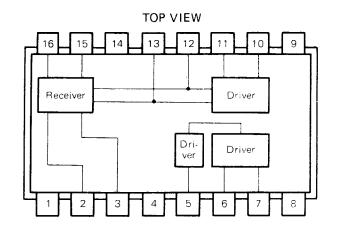
 CMP

 V

 1 2 3 4 5 6 7 8

- 1: INPUT2
- 2: OUTPUT2
- 3: OUTPUT2
- 4: OUTPUT1
- 5: OUTPUT1
- 6: VR
- 7: VAGC
- 8: VG (GND)
- 9: Vee
- 10: INPUT1
- 11: INPUT1
- 12: GA
- 13: GB
- 14: VBB
- 15: INPUT2
- 16: Vcc
- 1: OUT1
- 2: OUT1
- 3: IN2
- 4: IN2
- 5: VH
- 6: VL
- 7: SQ
- 8: GND
- 9: Vee
- 10: AGCG
- 11: CLA
- 12: CAP
- 13: VAGC
- 14: IN1
- 15: IN1
- 16: Vcc

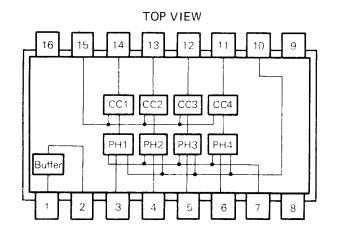
3) MB4316C Read/Write Bus Switch



1: Vee2 2: GAN2 3: GAN1 4: IN5 5: IN4 6: OUT5 7: OUT6 8: GND 9: Vee1 10: IN2 11: IN3 12: OUT4 13: OUT3 14: IN1

15: OUT2 16: OUT1

4) MB4319C Peak Hold

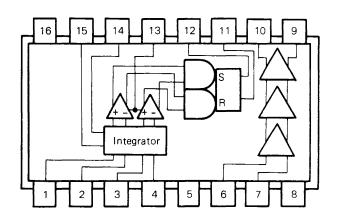


PH: Peak Hold

CC: Constant Current

- 1: REG1 2: VELOCITY 3: *GATE1 4: *GATE2
- 5: *GATE3 6: *GATE4
- 7: CARIE
- 8: GND
- 9: VEE 10: REG3
- 11: EVEN212: ODD2
- 13: EVEN1
- 14: ODD1
- 15: REG2
- 16: Vcc

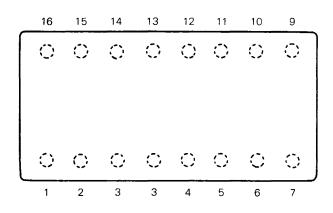
5) MB4320C Pulse Shaper



1: RDX1
2: RDX2
3: RDY1
4: RDY2
5: VEE
6: RDA
7: RDB
8: GND
9: OUT4
10: OUT3
11: OUT2
12: OUT1
13: VDX
14: CEY
15: CEX

16: Vcc

6) DV18 Clock Driver

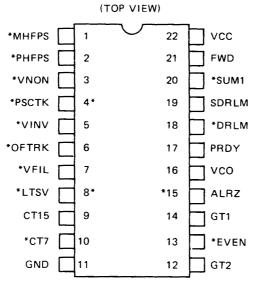


2: ENB
3: XE1
4: N.C.
5: N.C.
6: N.C.
7: XEZ
8: GND
9: N.C.
10: N.C.
11: N.C.
12: N.C.
13: OUT
14: N.C.
15: Vcc
16: N.C.

1: N.C.

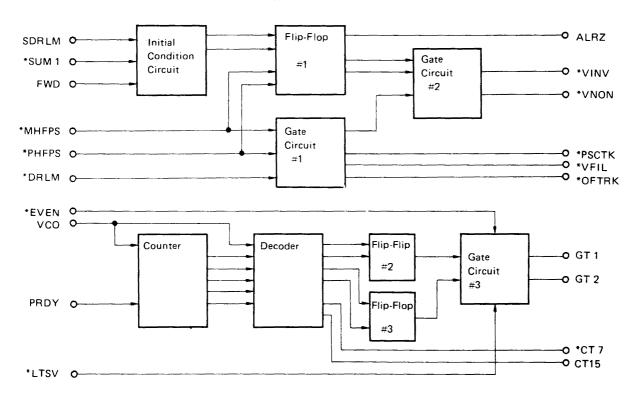
7) MB14601C Linear Motor Control

CONNECTION DIAGRAM



* NOT USED

BLOCK DIAGRAM



Section 9 Parts List

9. PARTS LIST

9.1 ASSEMBLY DRAWINGS (ILLUSTRATION)

The assembly drawing is the illustration that each part of every block was analyzed relationally on the assembly. Each analyzed part is given the number, which corresponds to the number in the INDEX No. column of the list. And mechanical assembly showing which part of the unit is analyzed, is given on the page.

NOTE) The parts that can't be disassembled on a usual maintenance work are not illustrated in their assembled state, and given a number of the parts. And the quantity of parts, and specification are entered in the list corresponding to the number of parts.

When all parts are entered in the list, the INDEX No. column will be blank.

9.2 LIST

The quantity of parts, the name of parts and specification are entered corresponding to the number of the illustration.

9.2.1 Index No.

A number is assigned on each part in the illustration. The number corresponds with the INDEX No. But in case INDEX No. is given at every part of assembly, the column of INDEX No. will be blank.

9.2.2 Composition & Quantity

Quantity of composition represents the major and minor relation to the setting No. of assembly parts. (The left side indicates large assembly, and the parts in the assembly shift to the right in turn).

9.2.3 Specification

Specifications of parts (drawing No.) are represented.

9.2.4 Description

Name of the part, manufacturer of parts and applicable machine are entered.

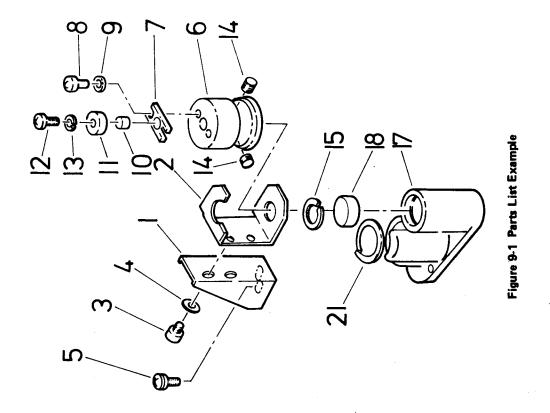
9.3 EXAMPLE

COMPOSITION & QUANTITY:

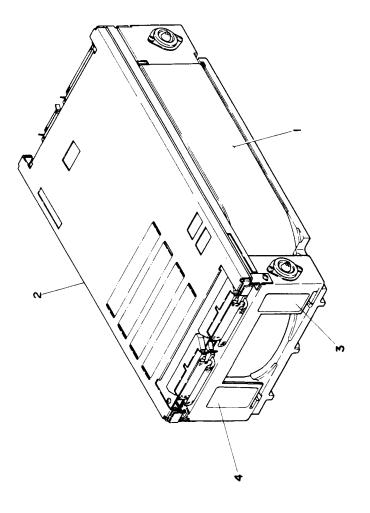
"B010-3110-T001A" consists of "B010-3110-V044A", "F6-SWINA-4 \times 10S" "B010-3110-V035A" and "F6-SAHT-4 \times 6" of these; "B010-3110-V044A" consists of 1-4 of the INDEX No. column, and "B010-3110-V035A" consists of 6-13.

The quantity of each part that is mounted is given by the number is this column.

Parts whose INDEX No. has *mark are maintenance parts.



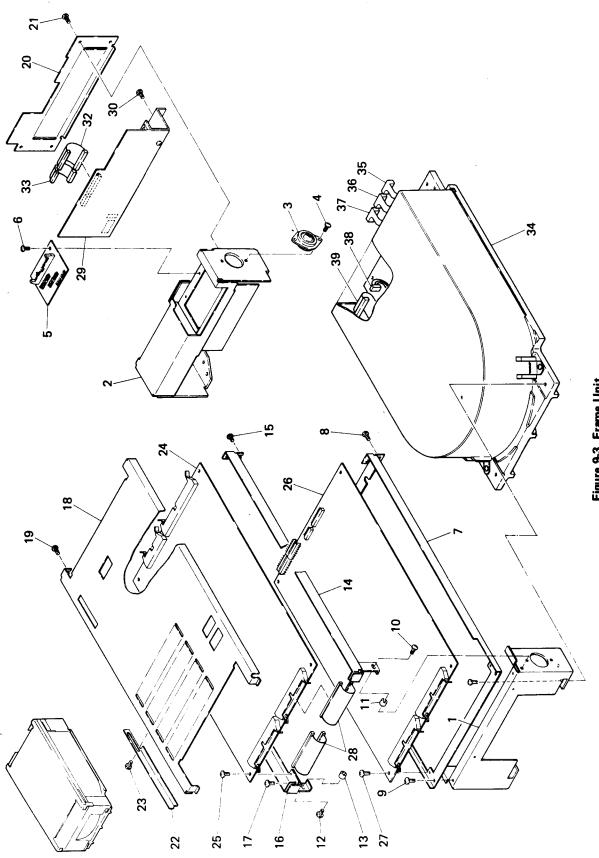
9-2



B03P-4590-0103A...B

Table 9-1 M2311K/M2312K Micro Disk Drive

INDEX NO.		COMP	OSIT	ION		SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1					B03B-4595-B001A	M2311K Micro Disk Drive		M2311K only	
	1	11				B03B-4595B002A	M2312K Micro Disk Drive		M2312K only	
1		1	}			B030-4590-T002A	M2311K Disk Drive Unit	·	M2311K only	
1		1				B030-4590-T001A	M2312K Disk Drive Unit		M2312K only	
2		1				B030-4590-V300A	Frame Unit			
3		1				C370-1270-0002	Manufacturing Name Label	·		
3		1				C370-1270-0002	Manufacturing Name Label			
4		1		.		C370-1270-0003	Revision Label			
4		1				C370-1270-0003	Revision Label			
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2

				Table 9-2 Frame	e Unit (1/2)		
INDEX NO.		POSITION	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1		B030-4590-V300A	Frame Unit			
1	1		B030-4590-Y022A	Plate	•		
2	1	1 1 1 1	B030-4590-W011A	Plate Assy.			
3	4		B30L-2670-0001A	Rubber Vibration Isolation			
4	8		F6-SBD-4x6S	Screw			
5	1 1		B16B-7920-0010A	Through Connector	TINM		
6	2		F6-SW2NA-3x6S	Screw			
7	1 1		B030-4590-Y020A	Frame			
8	2		F6-SBD-4x6S	Screw			
9	2		F6-SBD-4x6S	Screw			
10	1		F6-SBD-4x8S	Screw			
11	1		F6-SPK-4x4S	Spacer			
12	1	1	F6-SBD-4x8S	Screw			
13	1 1		F6-SPK-4x4S	Spacer			
14	1	1 1 1	B030-4590-W010A	Plate Assy.			
15	2		F6-SBD-4x6S	Screw			
16	1	1	B030-4590-W012A	Plate Assy.			
17	2		F6-SBD-4x6S	Screw			
18	1		B030-4590-X026A	Cover			
19	2	1 1 1	F6-SBD-4x6S	Screw	,		
20	1 1		B030-4590-X038A	Cover			
21	4		F6-SBD-4x6S	Screw			
22	1		B030-4590-X043A	Stay			
23	1		F6-SBD-3x6S	Screw			
24	1		B16B-6970-0010A#U	Controller A	CNAM		

CMZM

TUZM

Screw

Screw

Cable

Screw

Controller Z

Power Amplifier Z

Connection Cable

Connection Cable

F6-SBD-3x6S B16B-6960-0010A#U

F6-SBD-3x6S

F6-SBD-4x8S

B660-1065-T037A

B660-0625-T318A

B660-0625-T319A

B16B-7640-0010A#U

Table 9-2 Frame Unit (2/2)

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
34 34	1	B030-4590-T002A B030-4590-T001A	M2311K Disk Drive Unit M2312K Disk Drive Unit		M2311K only M2312K only	
35		B860-1520-V111A	Cable from Positioner Assy.		WIZO TZK OTTY	
36	1 1	B860-1520-V112A	Cable from Positioner Assy.			
37		B860-1520-V113A	Cable from Positioner Assy.			
38	1 1	C63L-0670-0013	Cable from Positioner Assy.			
39		B90L-1415-0100A	Cable from DC Motor			

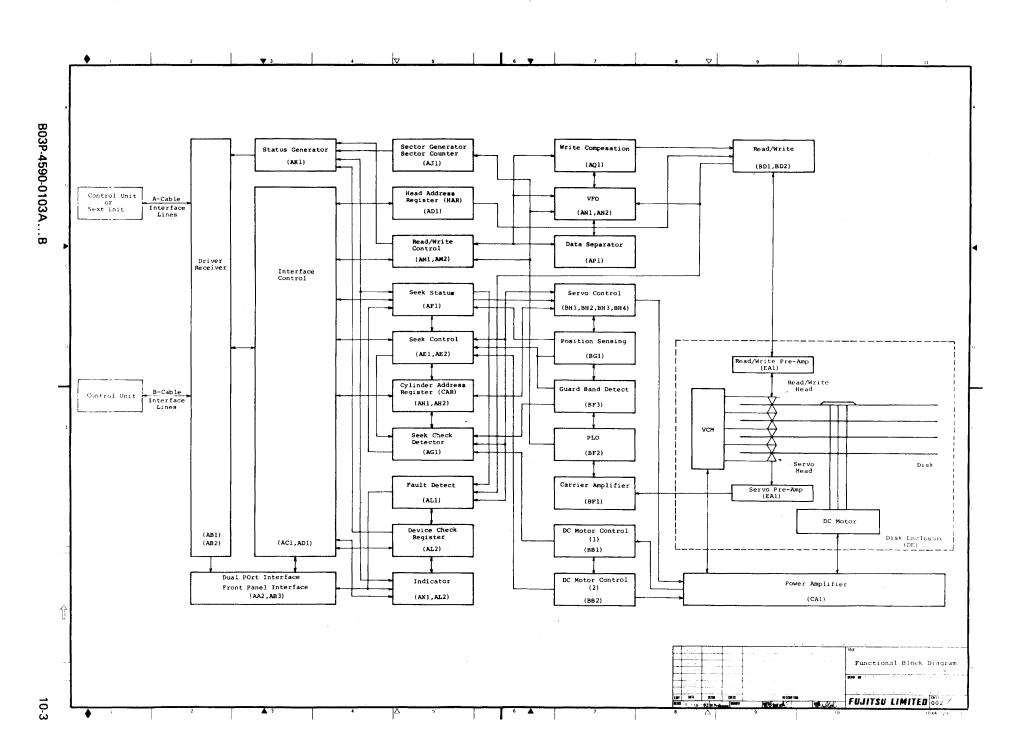
Section10 Schematics

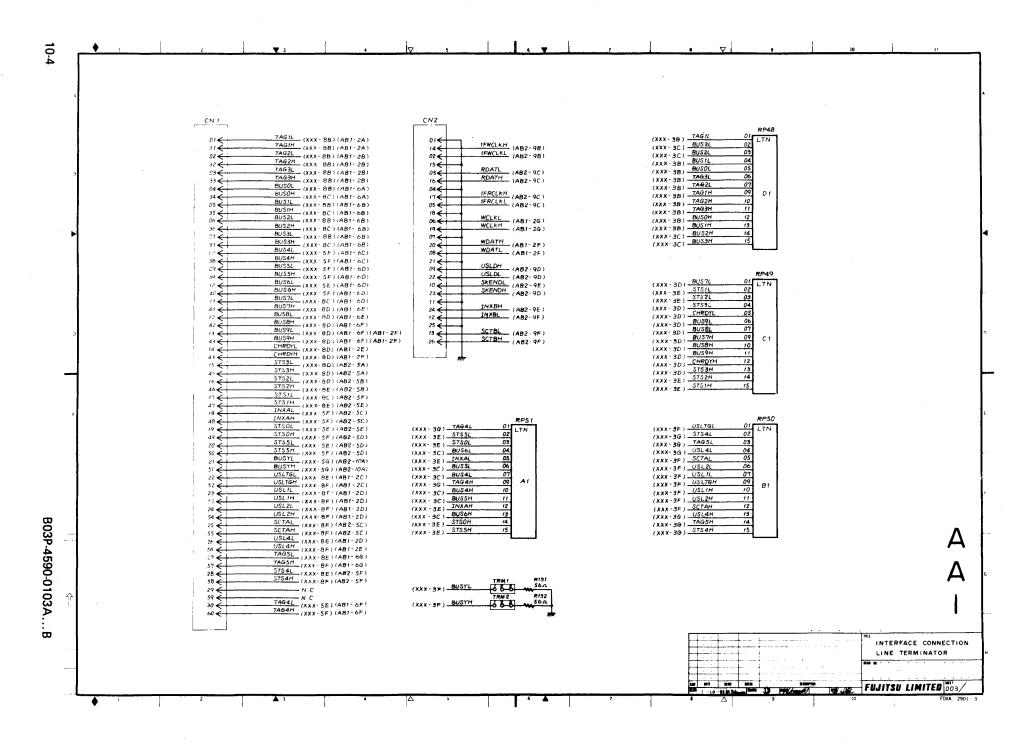
10. SCHEMATICS

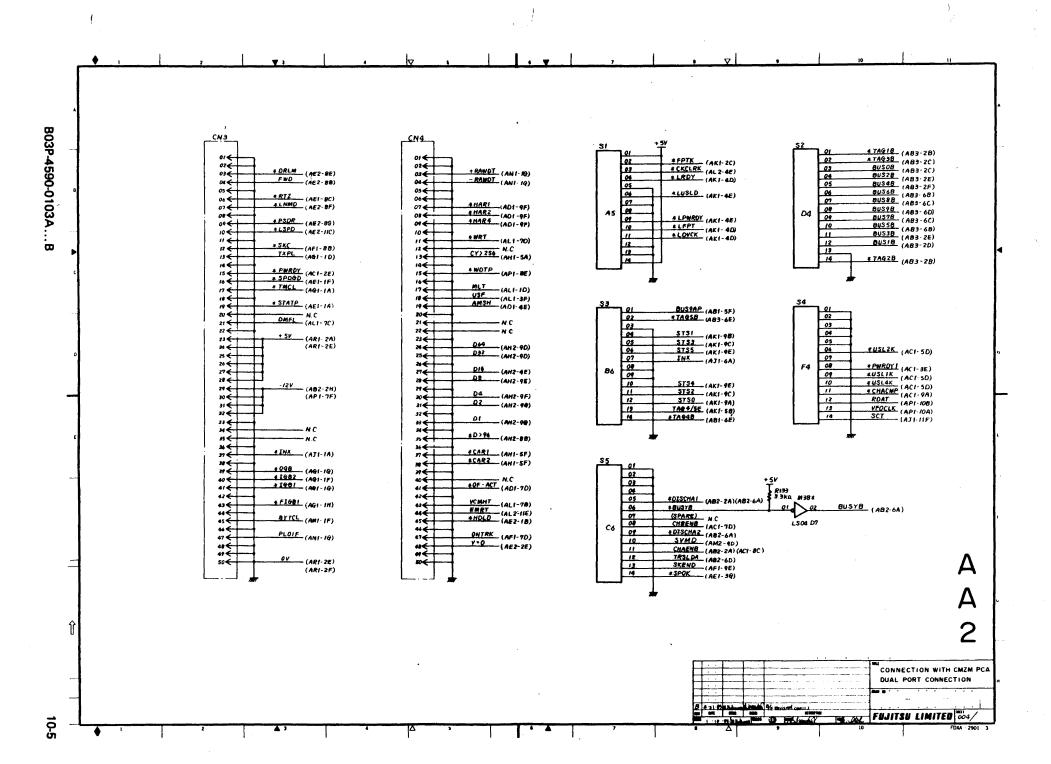
10.1 BASIC SCHEMATICS

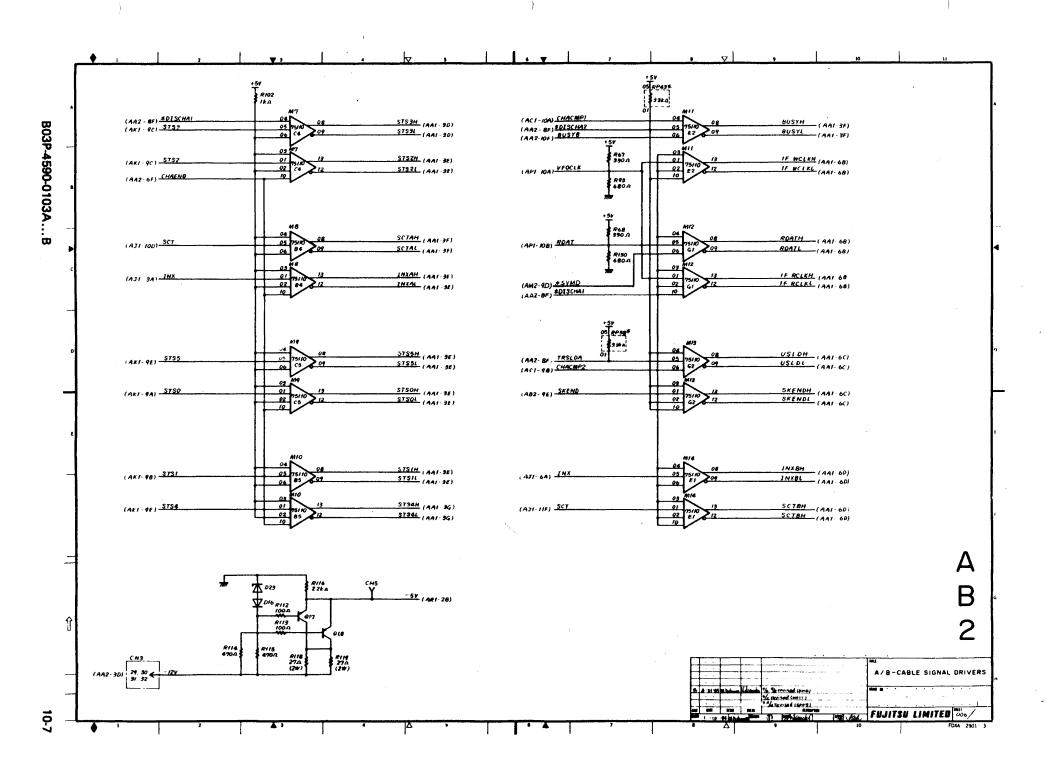
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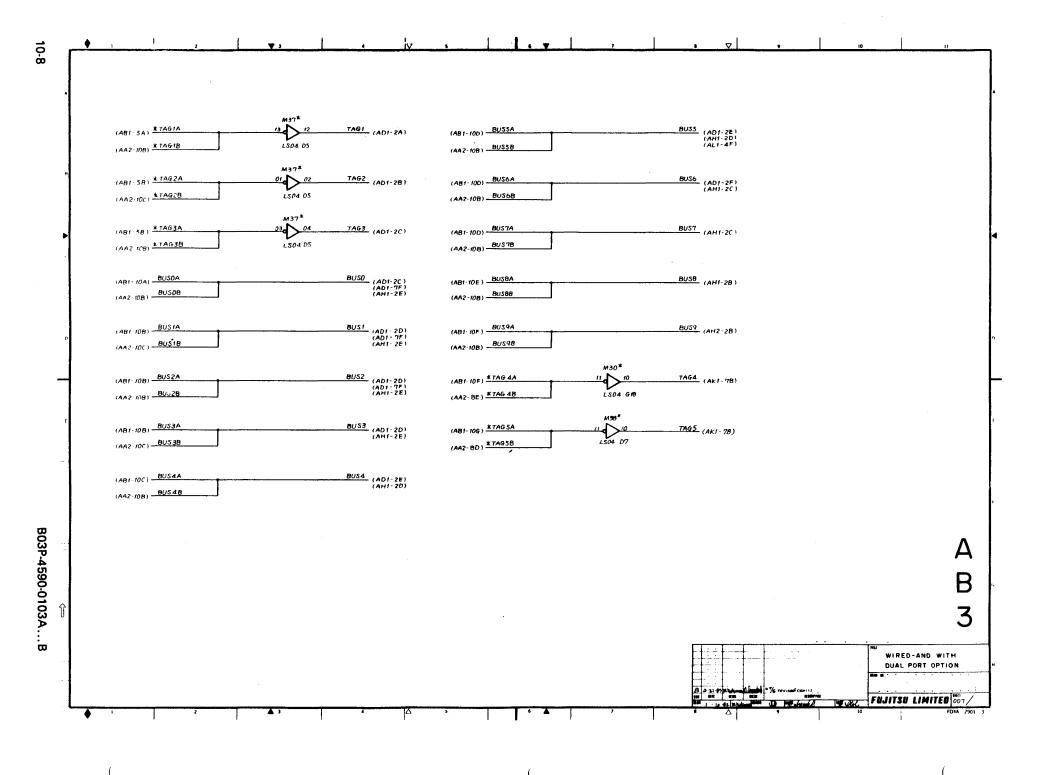
SHEET	ABBR	TITLE	SHEET	ABBR	TITLE	Τ						
001		Schematics/Drawings List	026	ARl	IC Power Supply	 						
002		Functional Block Diagram	027	BAl	Connction with CNAM, TINM and TUZM PCA's	 		1				
003	ΛAl	Interface Connection Line Terminator	028	BB1	DC Motor Control (1)	 					-	
004	AA2	Connection with CMZM PCA Dual Port Connection	029	BB 2	DC Motor Control (2)	1						
005	ABl	A-Cable Signal Receivers	030	BCl	Power Ready Detector	1	 					
006	AB2	A/B-Cable Signal Receivers	031	BDl	Read/Write Bus Switch Head and Chip Selections							
007	AB 3	Wired-AND with Dual Port Option	032	BD2	AGC Amplifier Pulse Shaper		 					
800	AC1	Unit Selection	033	BE1	HIC Power Supply	 	 					
009	ADl	Command Decoder Head Address Register (HAR)	034	BFl	Carrier Amplifier PLO Phase Comparator	-	<u> </u>					
010	AE l	Seek Control Latches (1)	035	BF2	PLO Charge Pump and VCO	 						
011	AE 2	Seek Control Latches (2)	036	BF3	Guard Band Detect	†	<u> </u>					
012	AFl	Seek Status Generator	037	BG1	Position Sensing	\dagger						
013	AG1	Seek Check Detector	038	BH1	Velocity Generator Fine Position Detect	-						
014	AH 1	Next/Present Cylinder Address Register (NCAR/PCAR)	0 39	вн2	DAC and Error Amplifier	†	<u> </u>					
015	AH2	Difference Counter	040	вн 3	Servo Power Amplifier Drive	 	 					
016	AJ1	Sector Generator Sector Counter	041	Вн 4	Servo Control Logic	t						
017	AK 1	Status Multiplexer LED Drivers	042	CAl	Servo Power Amplifier DC Motor Power Amplifier	 	<u> </u>					
018	ALl	Fault Detect	043	DAl	Connection with CMZM PCA and HIC	<u> </u>						
019	AL2	Fault Register and Indicators	044	EAl	Data/Servo HIC's	<u> </u>						\neg
020	AM1	VFO Control (1)	045	FAl	I/O Connectors of all PCA's							
021	AM2	VFO Control (2)	046		CNAM PCB Assembly					***************************************		
022	AN 1	VFO Phase Comparator	047		CMZM PCB Assembly	†						
023	AN 2	VFO Charge Pump and VCO	048		TUZM PCB Assembly	†						
024	AP1	VFO Data Separator	049		TINM PCB Assembly							
025	AQ1	Write Compensation and MFM Coding	1									
					B 4-21.45 M 7:45 mg 1 Limber 1973	in the second se	2-01/49 04/4 05 ,060/4 06/4 00	(g. 00/g 00/g 00/g 0	1810 00 ·	matics/I	Drawing	gs List

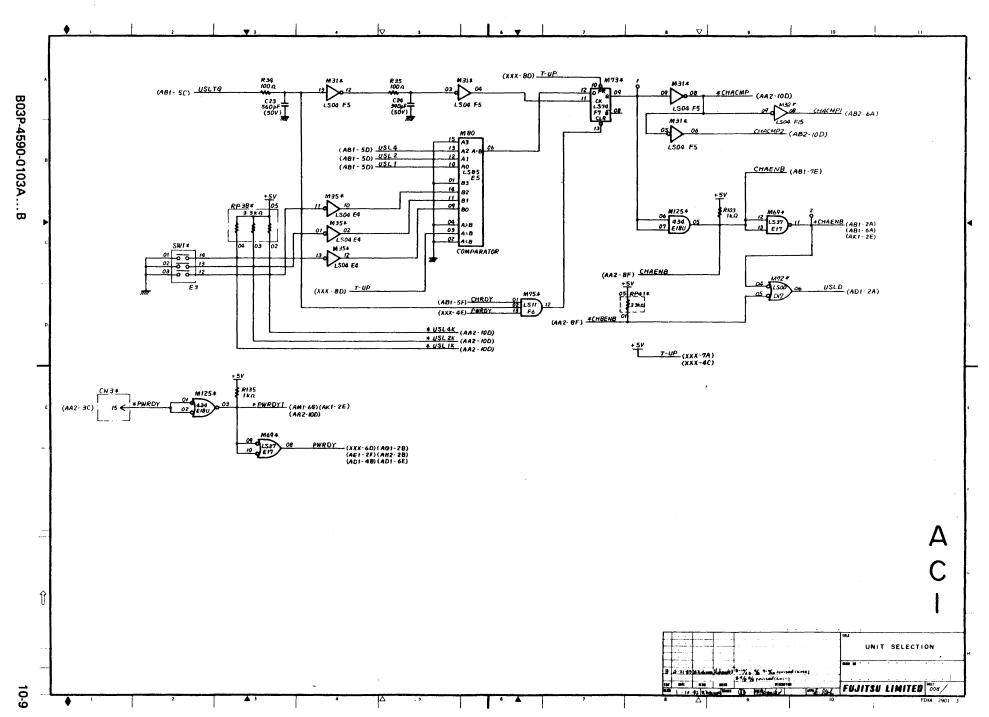




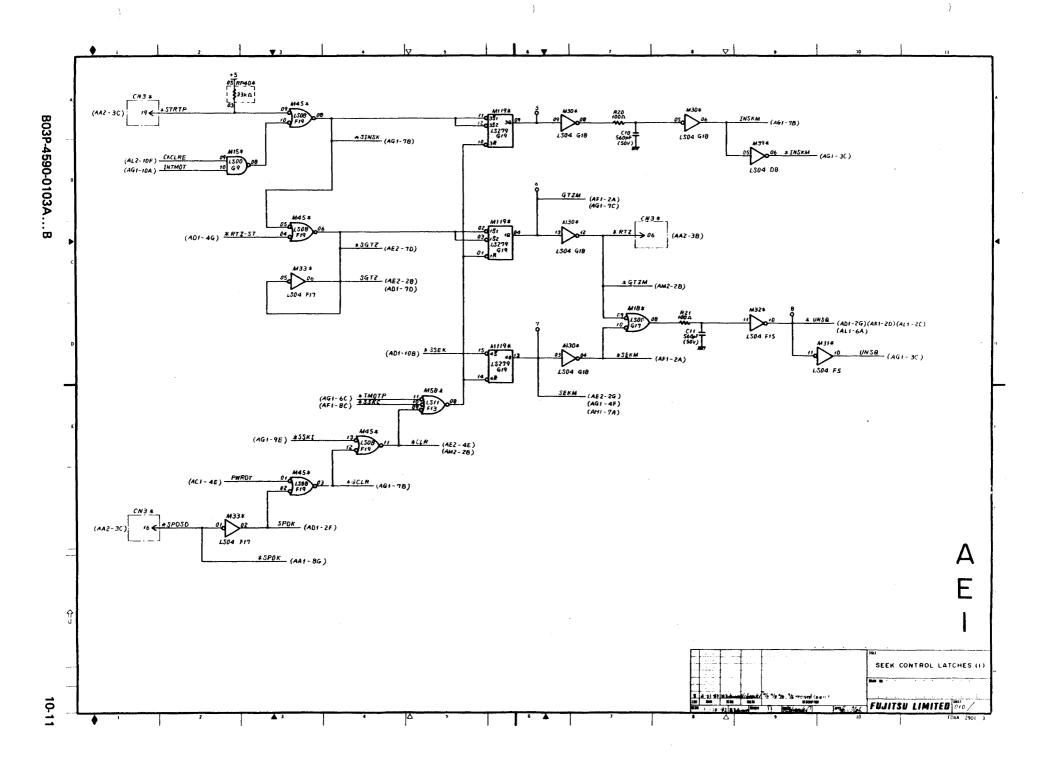


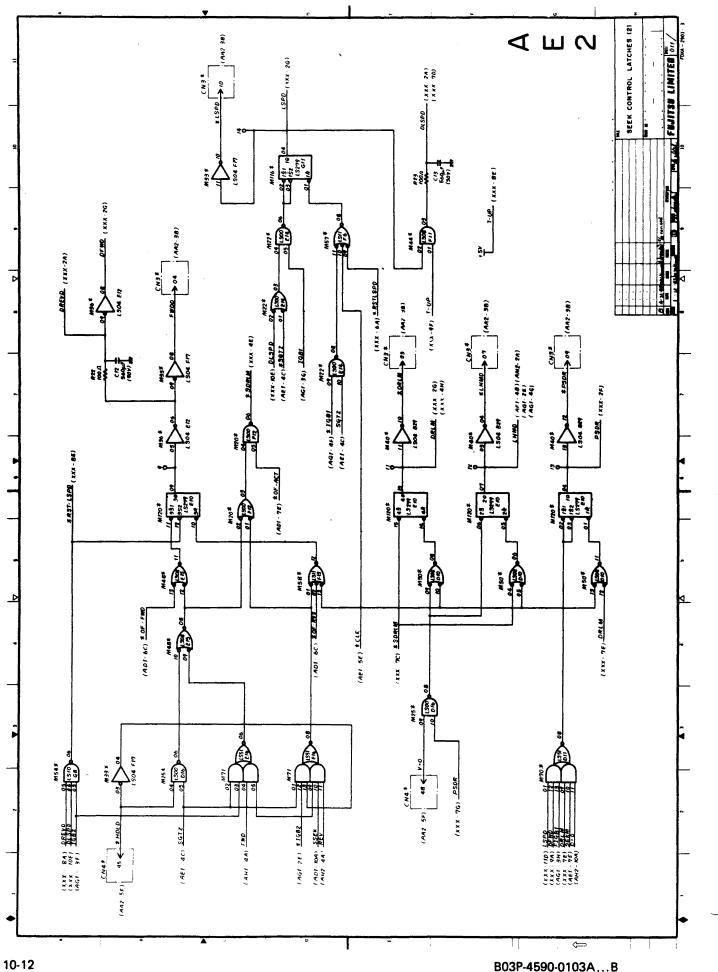


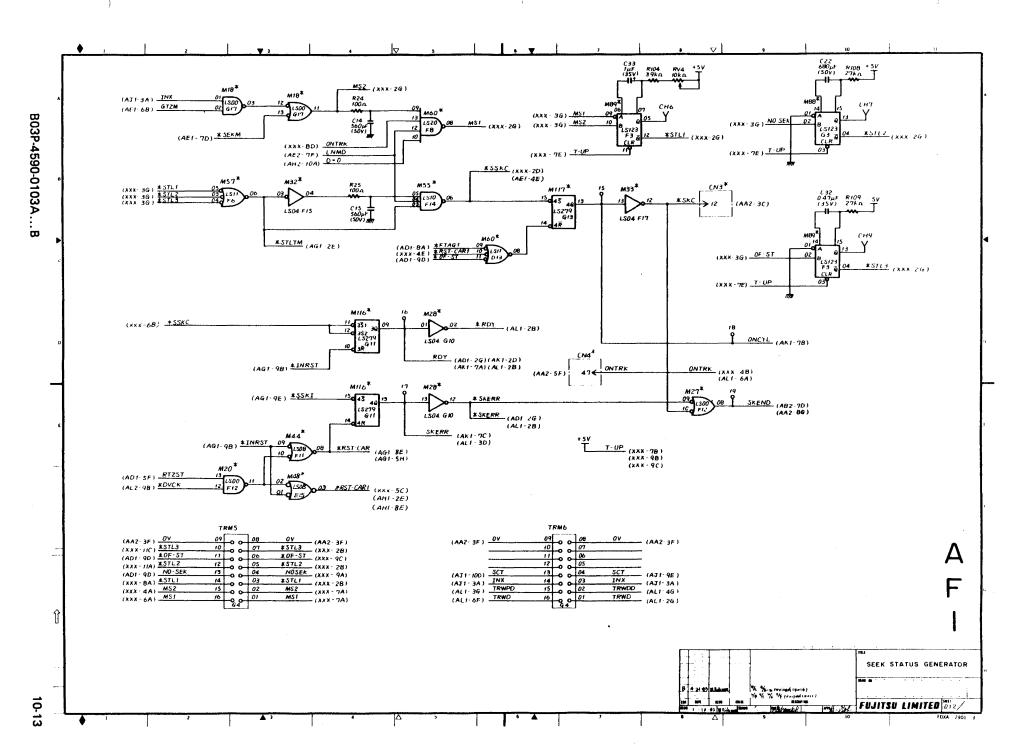


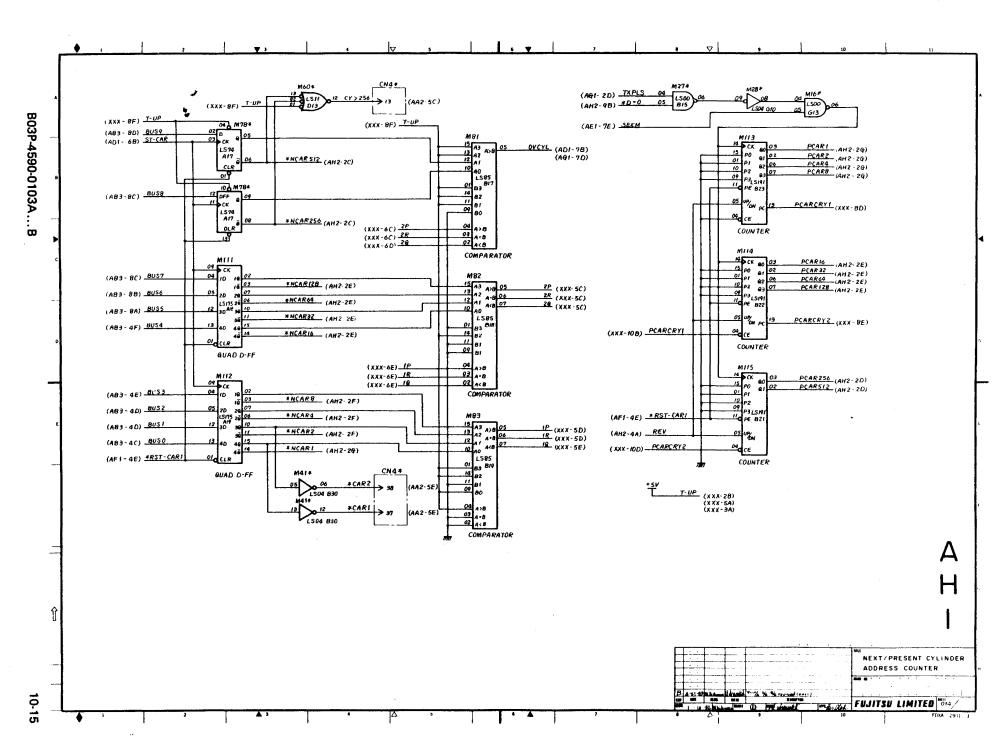


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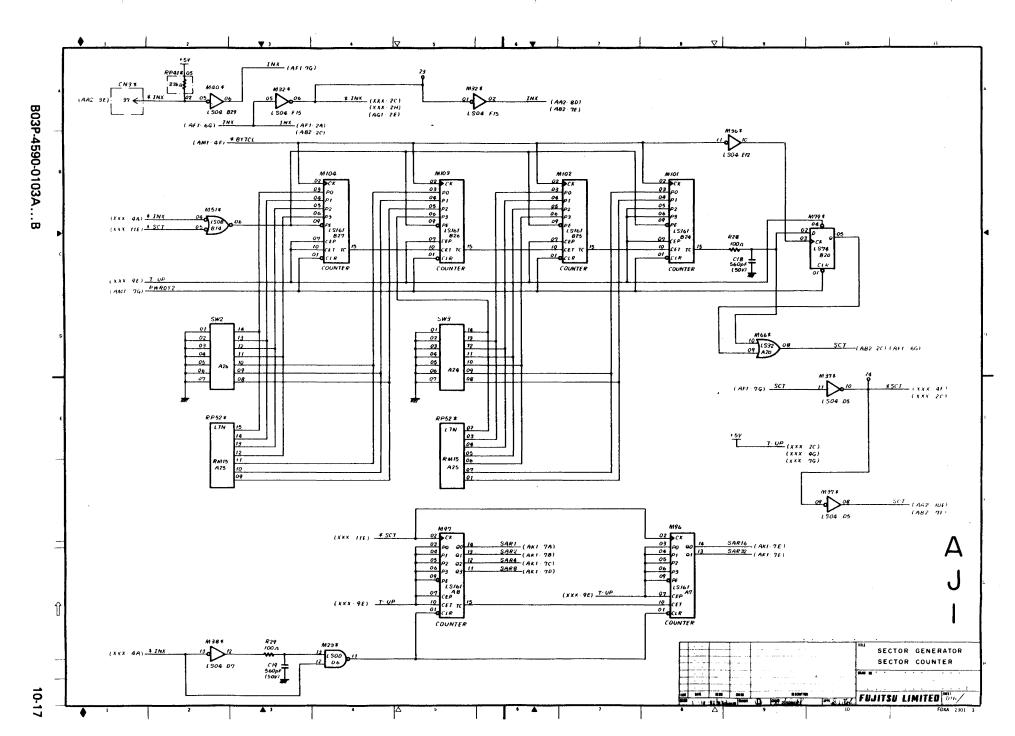


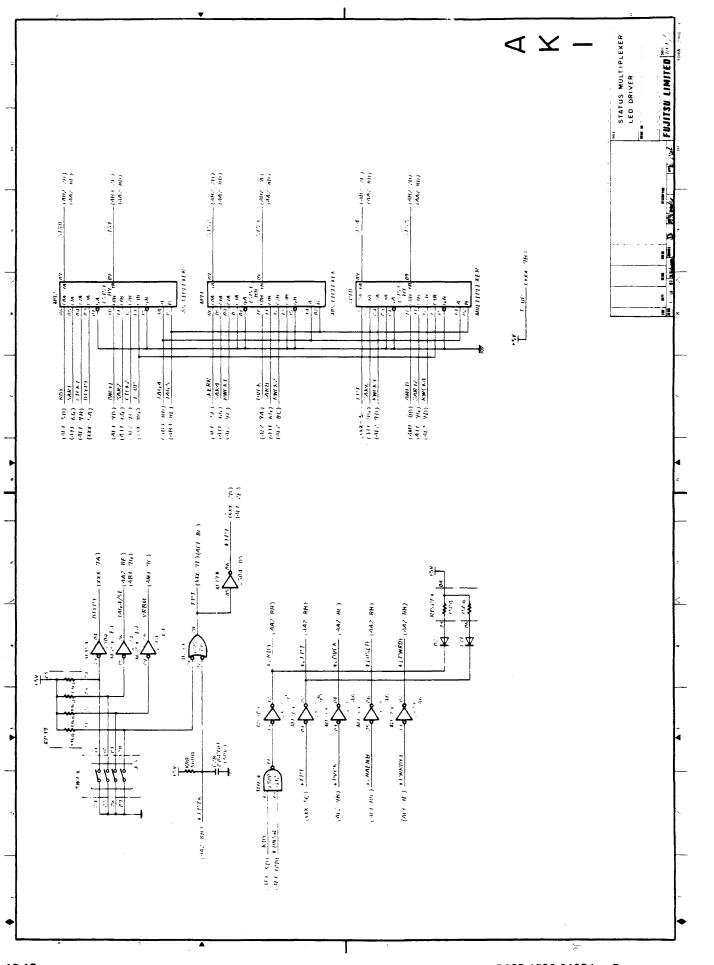


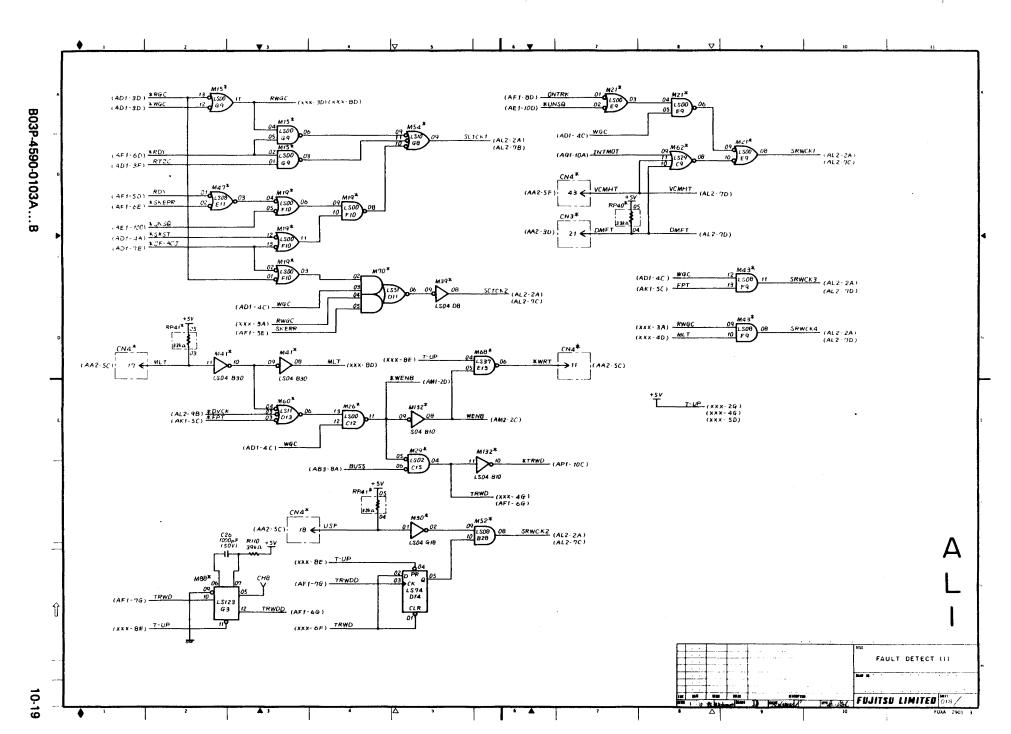


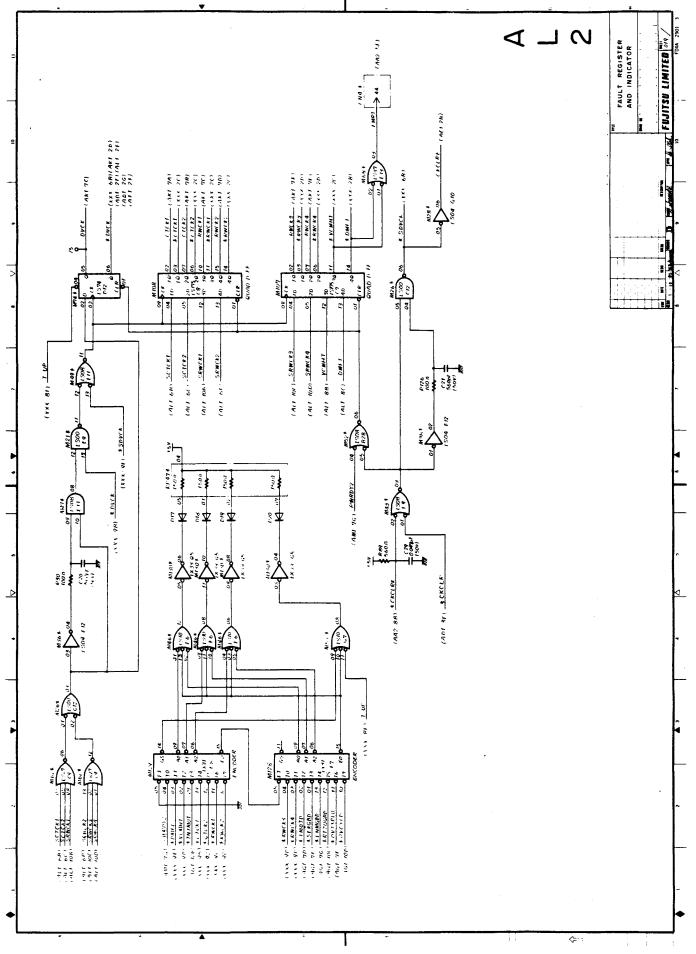


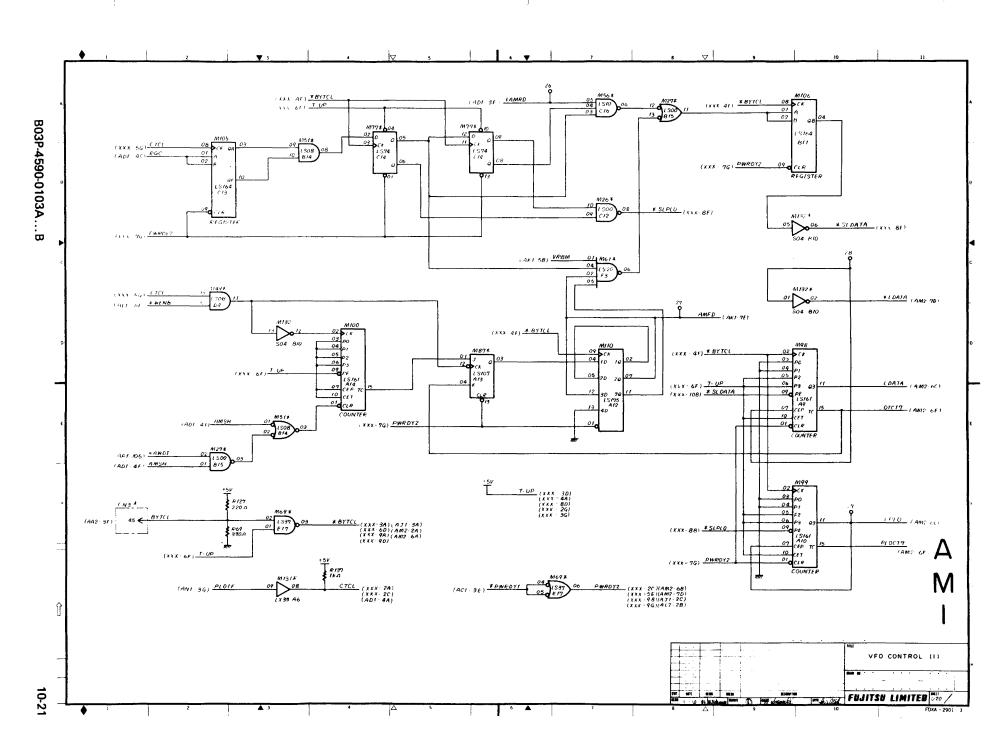
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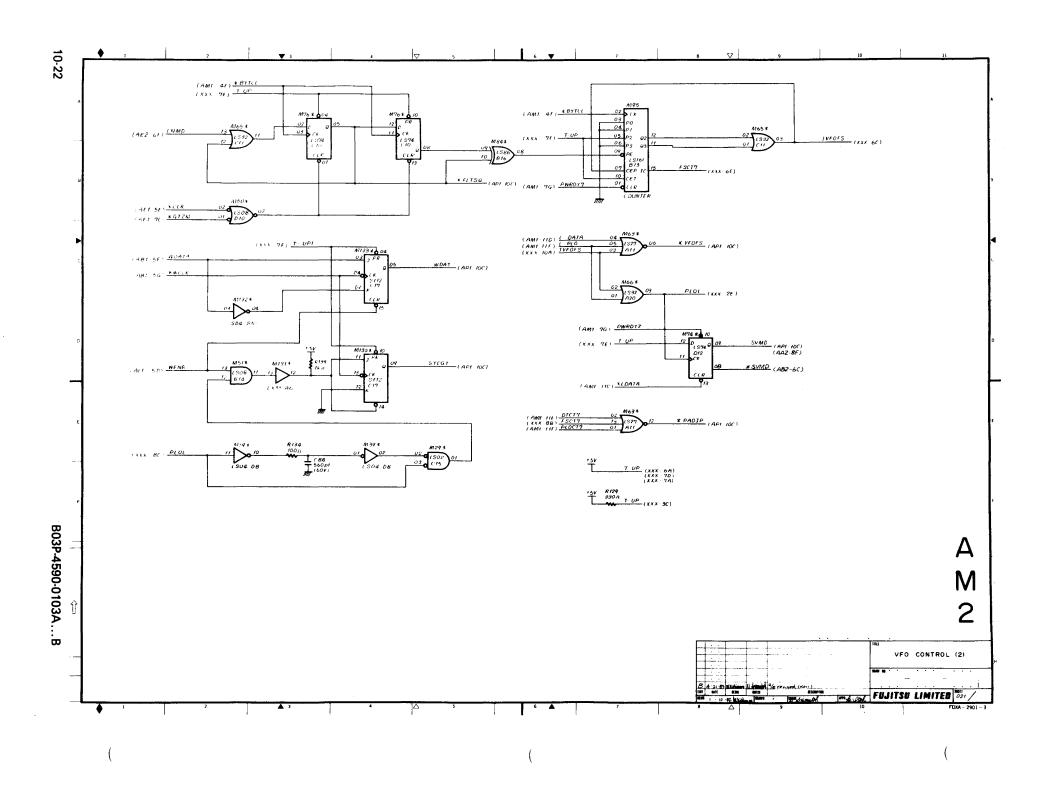


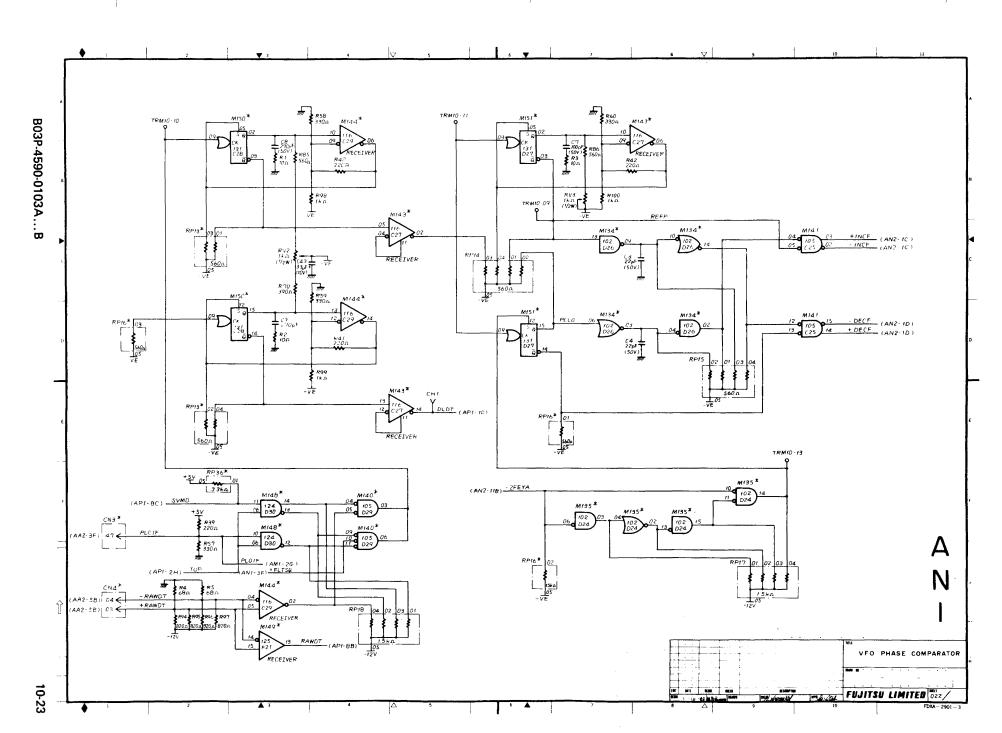




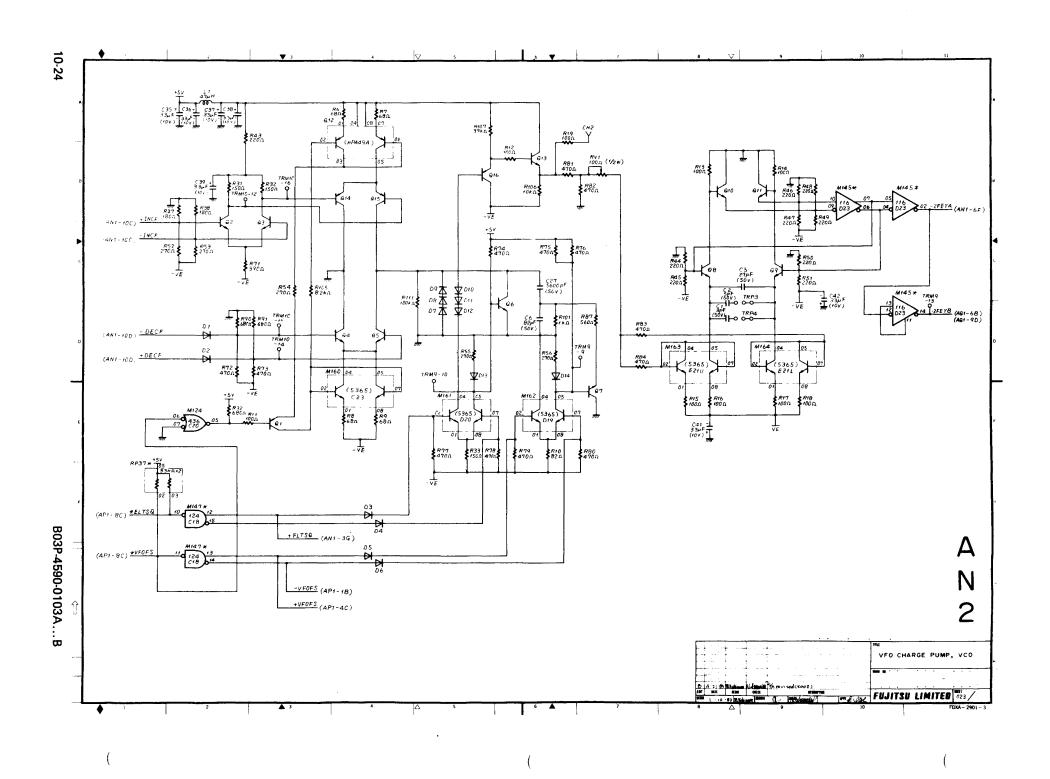


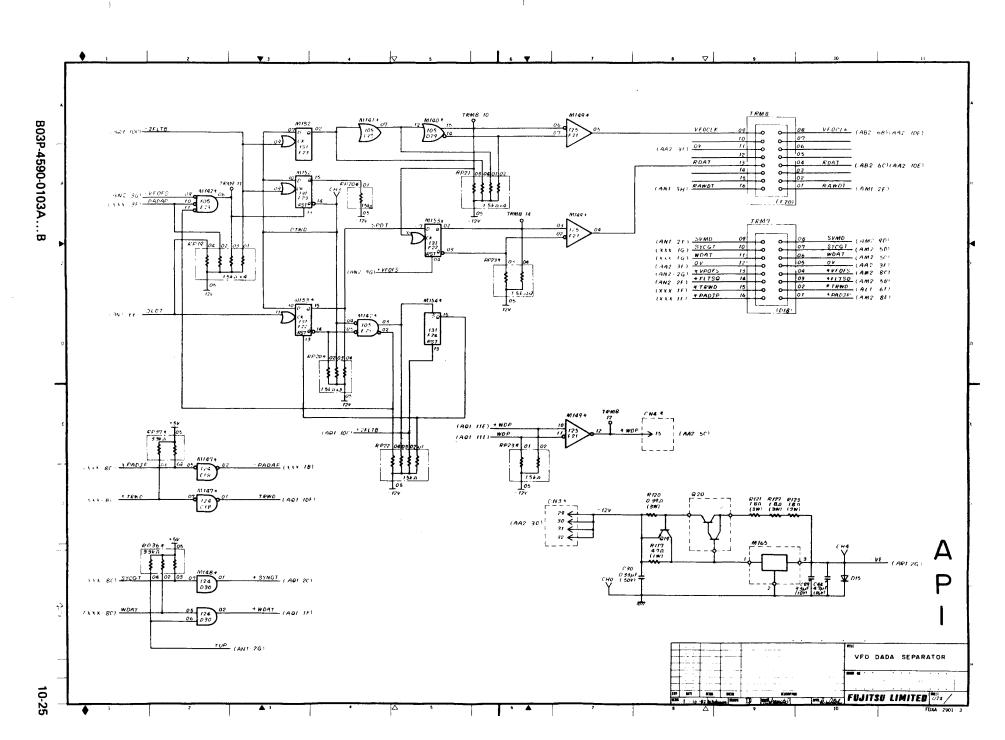
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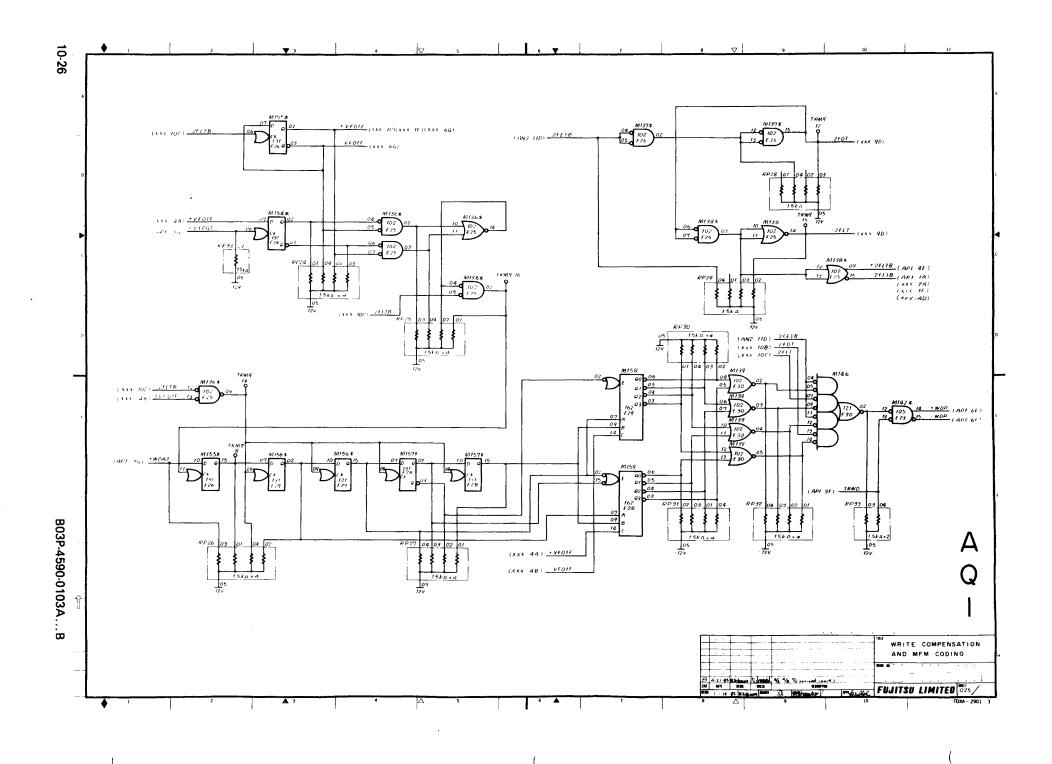


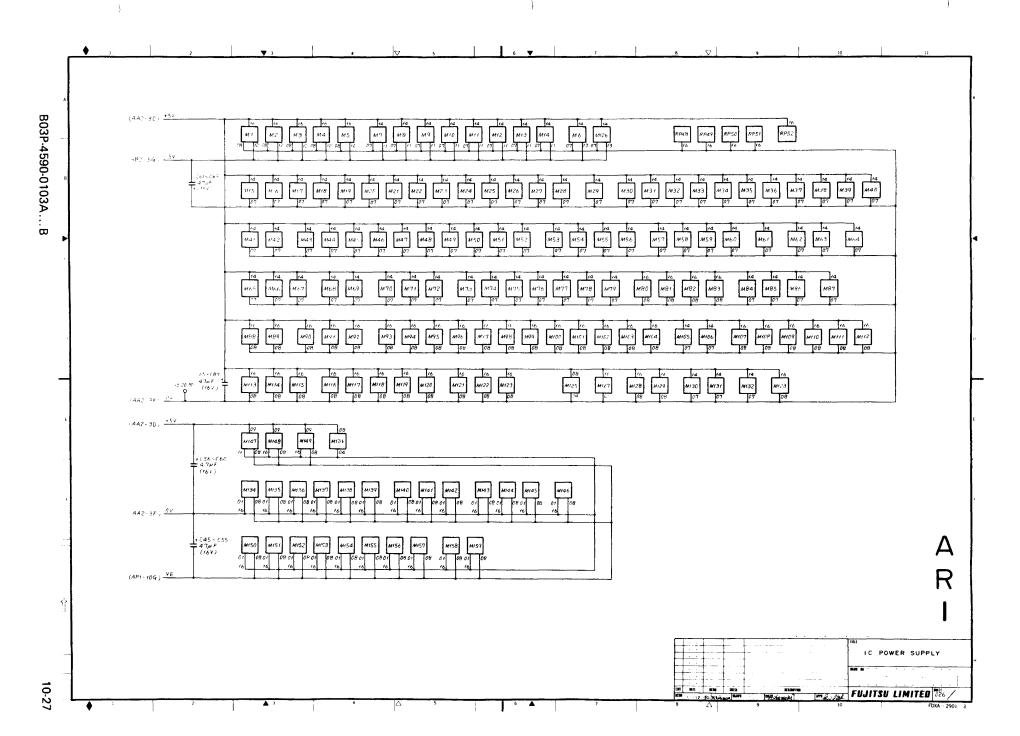


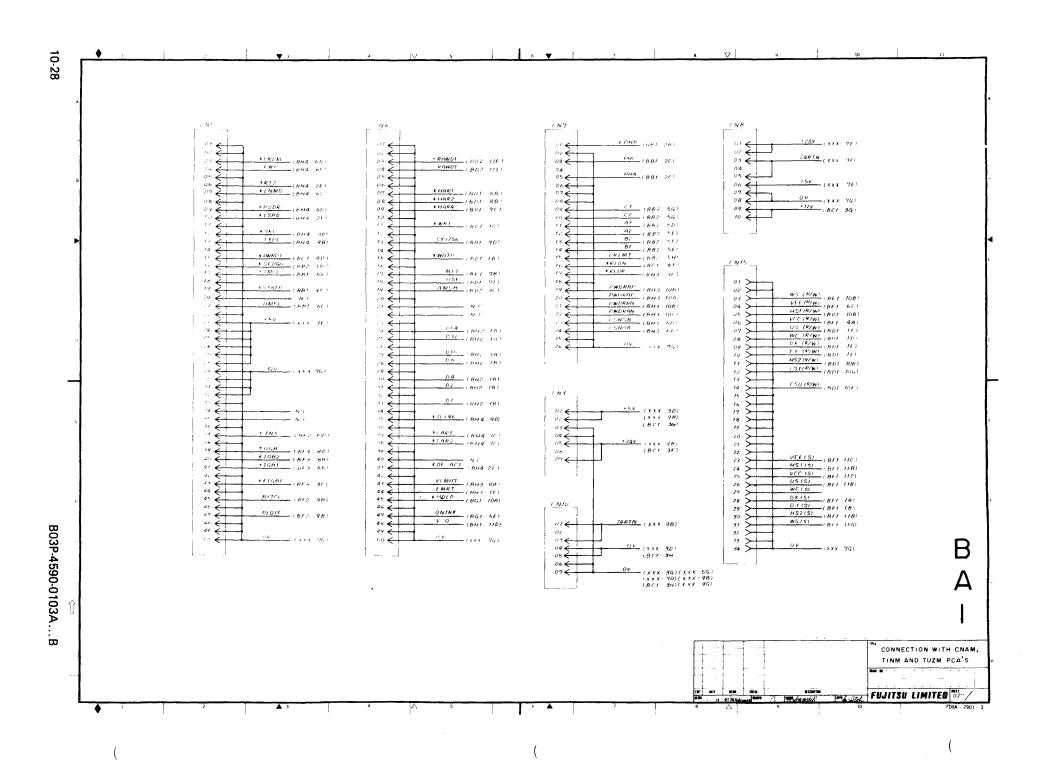
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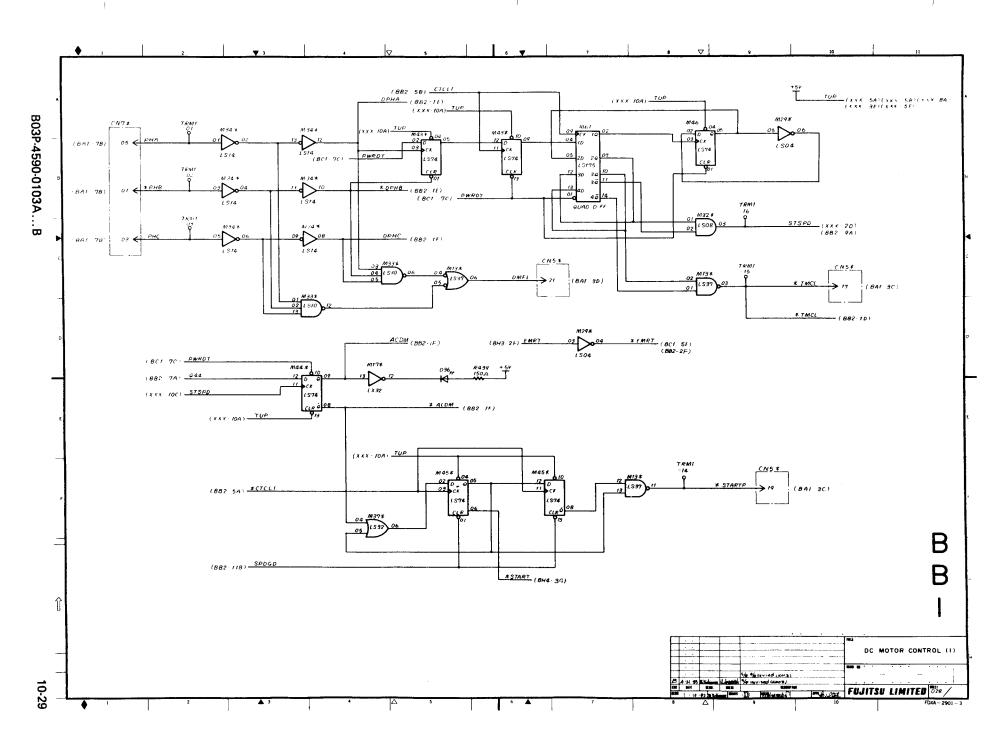


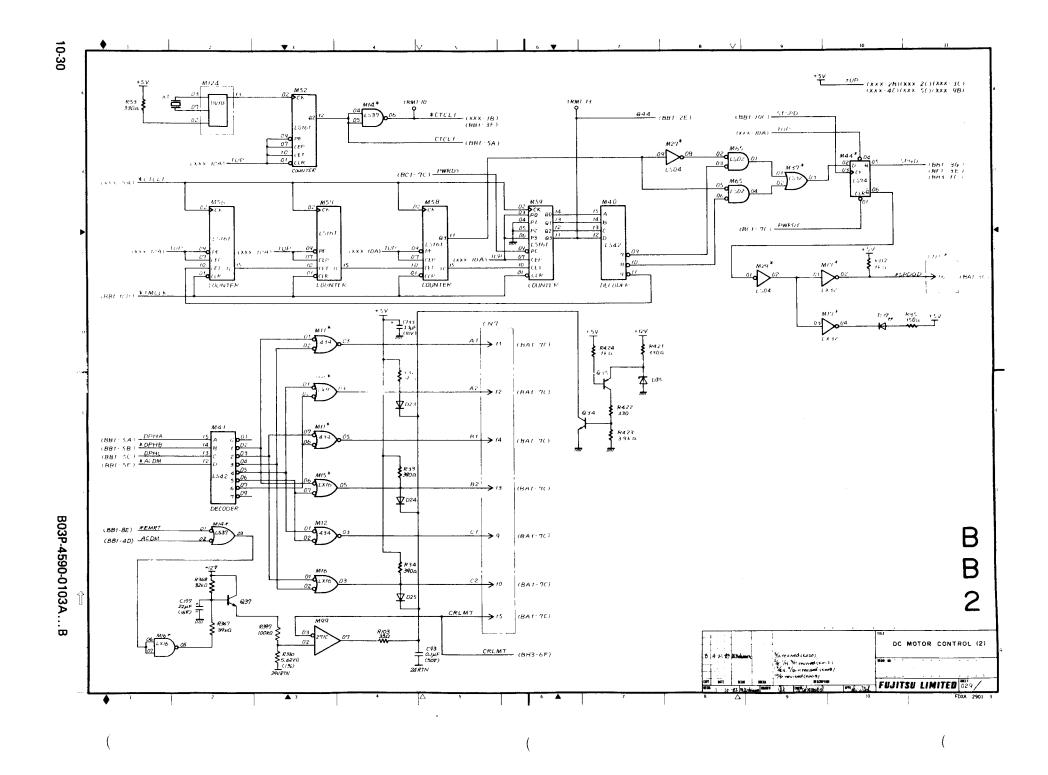


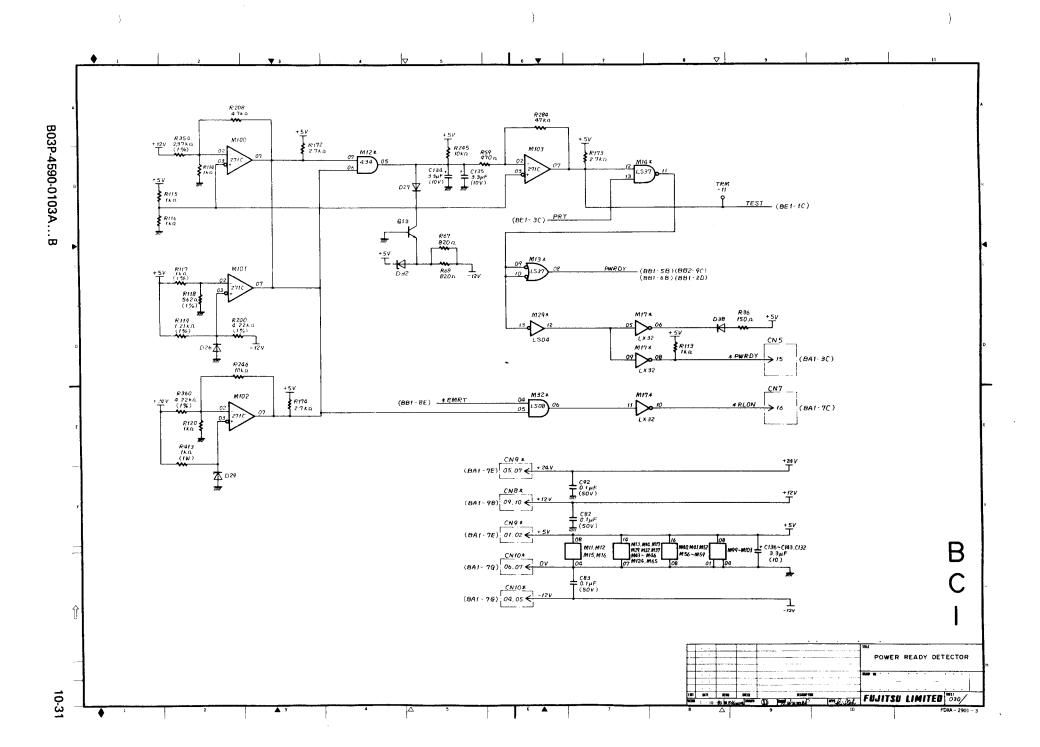


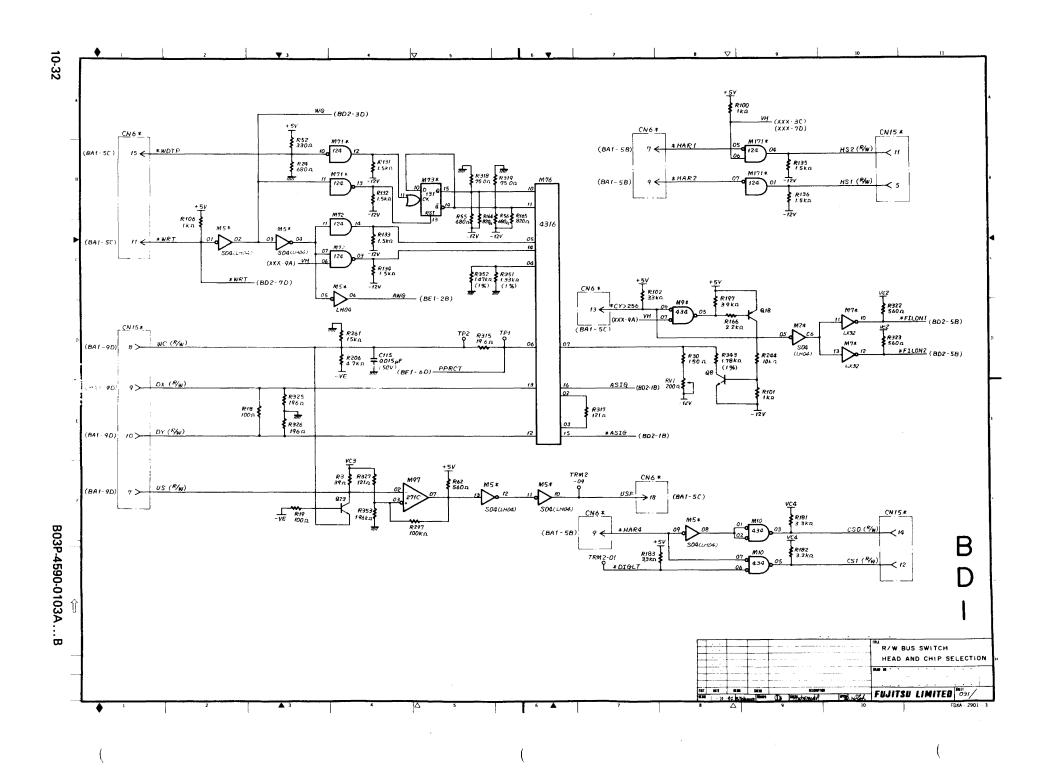


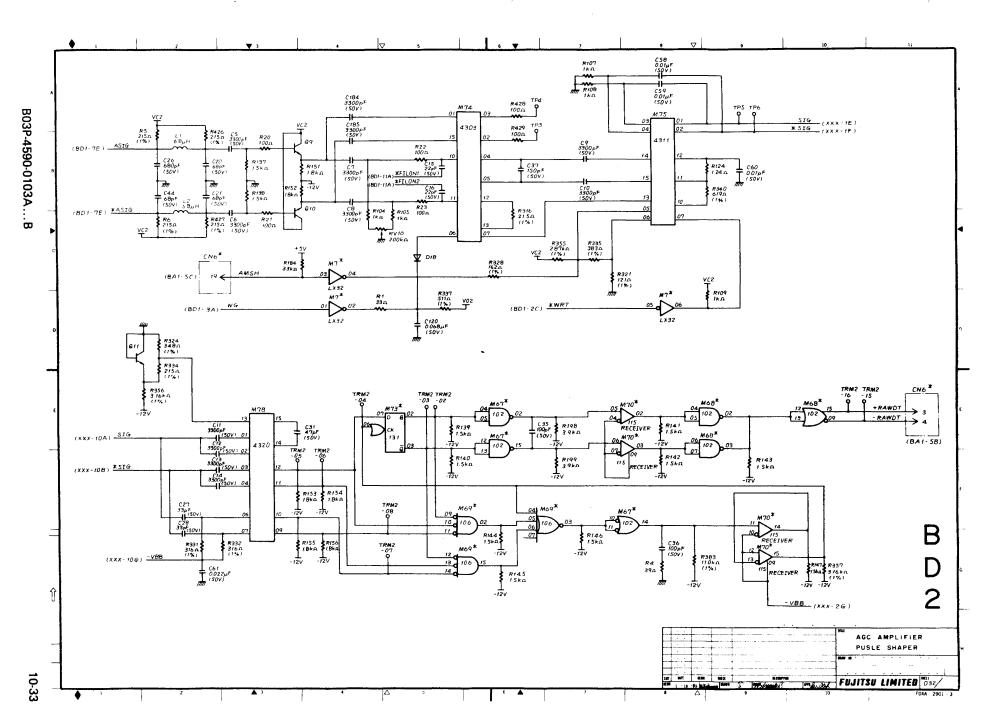




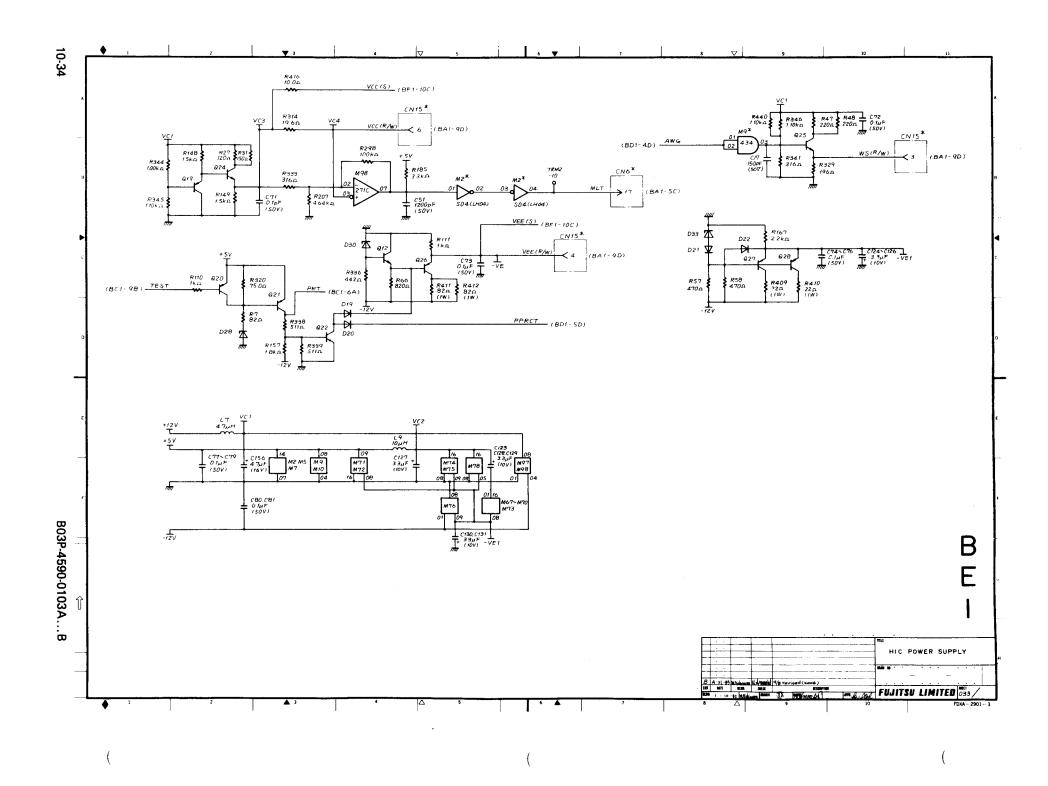


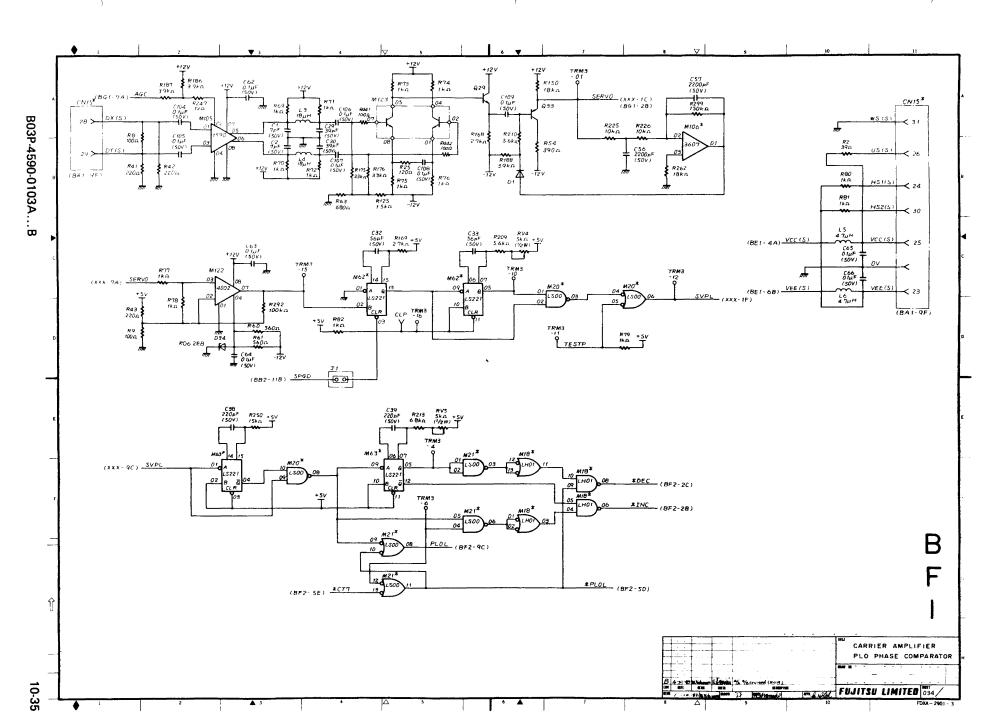


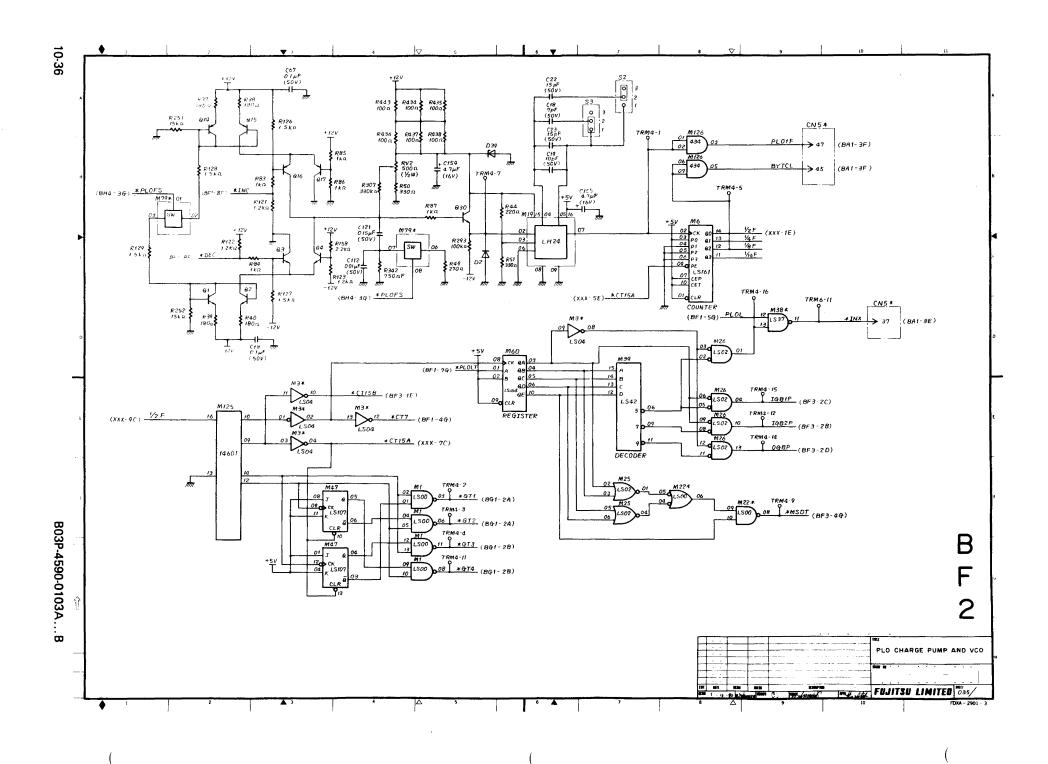


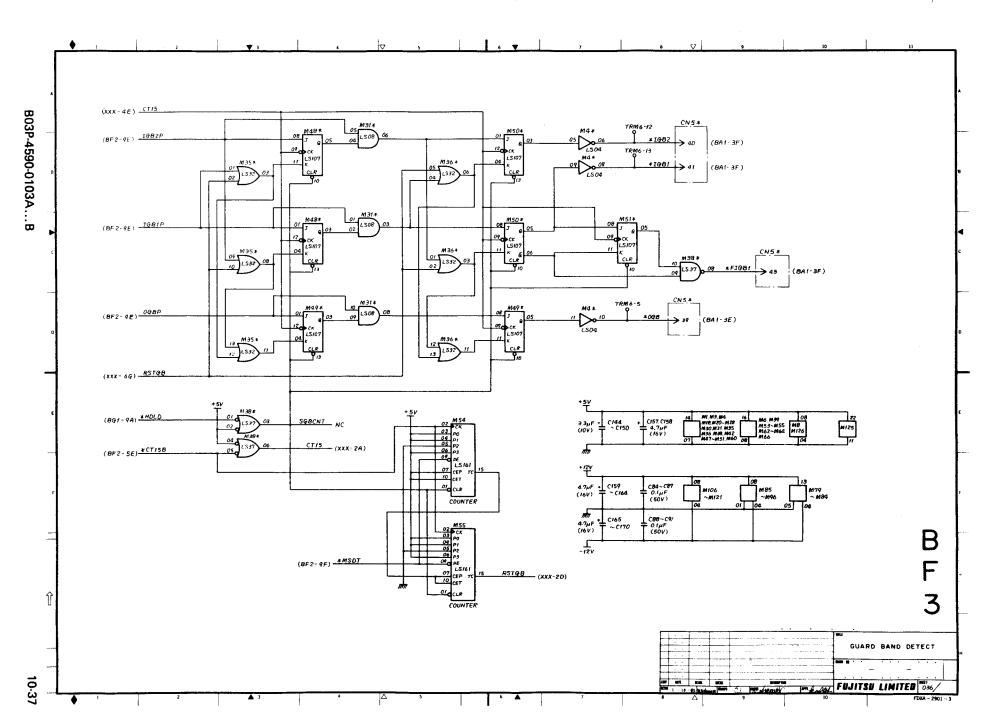


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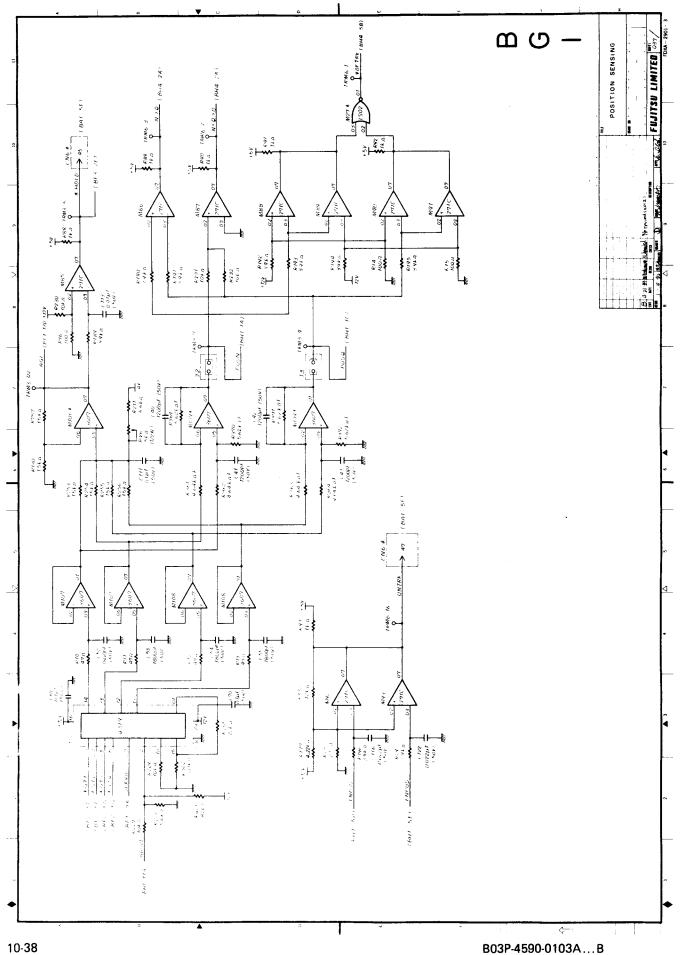


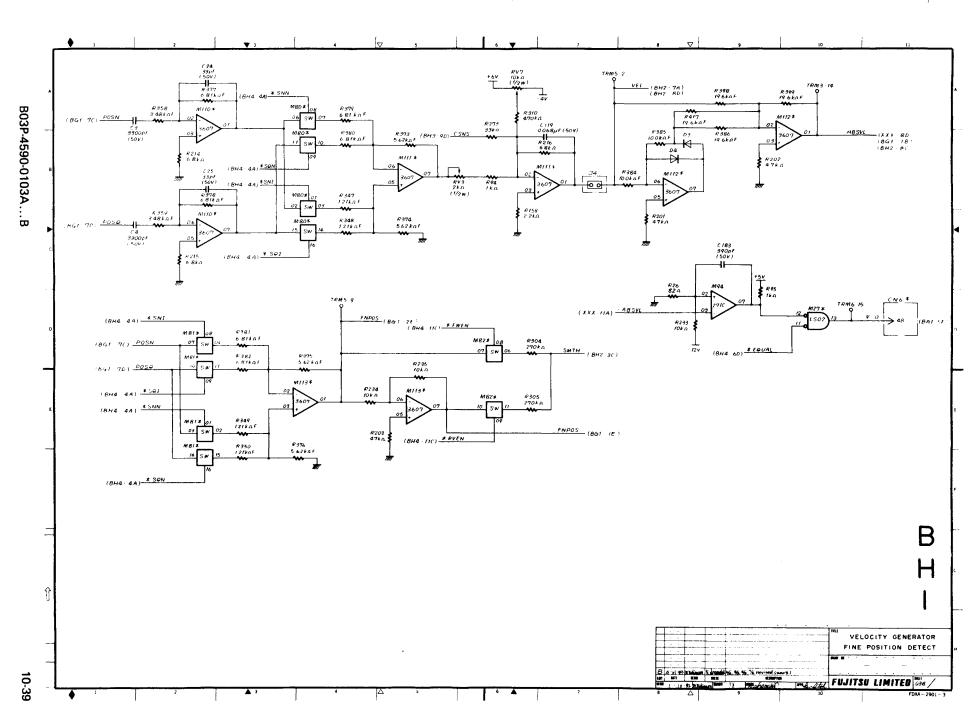




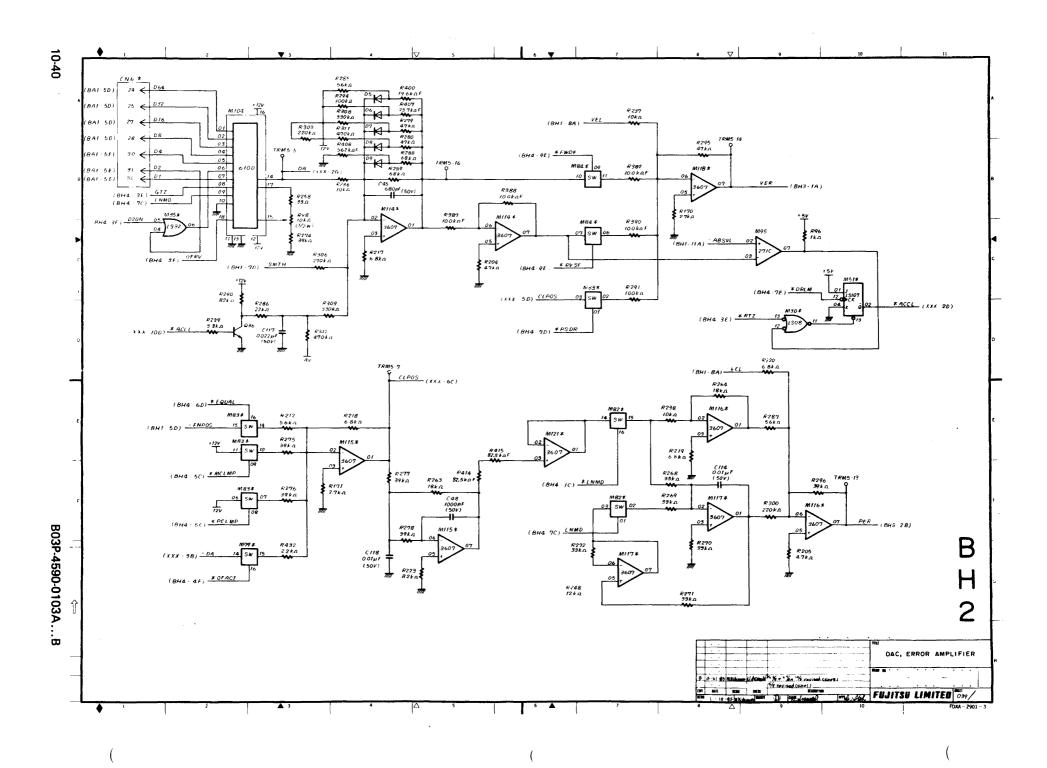


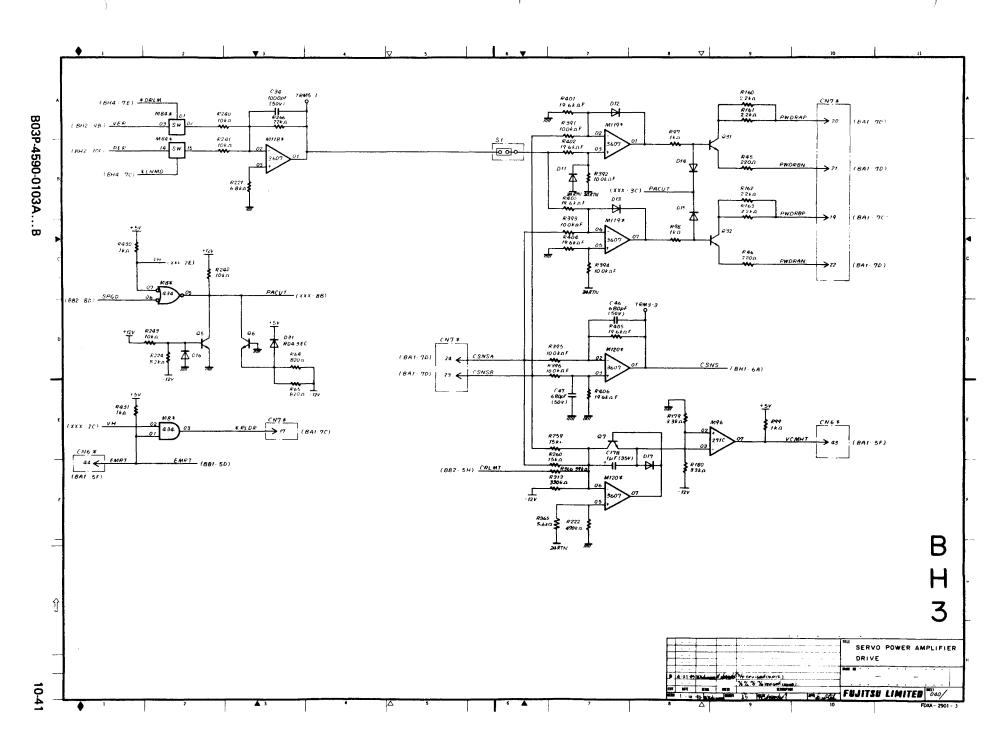
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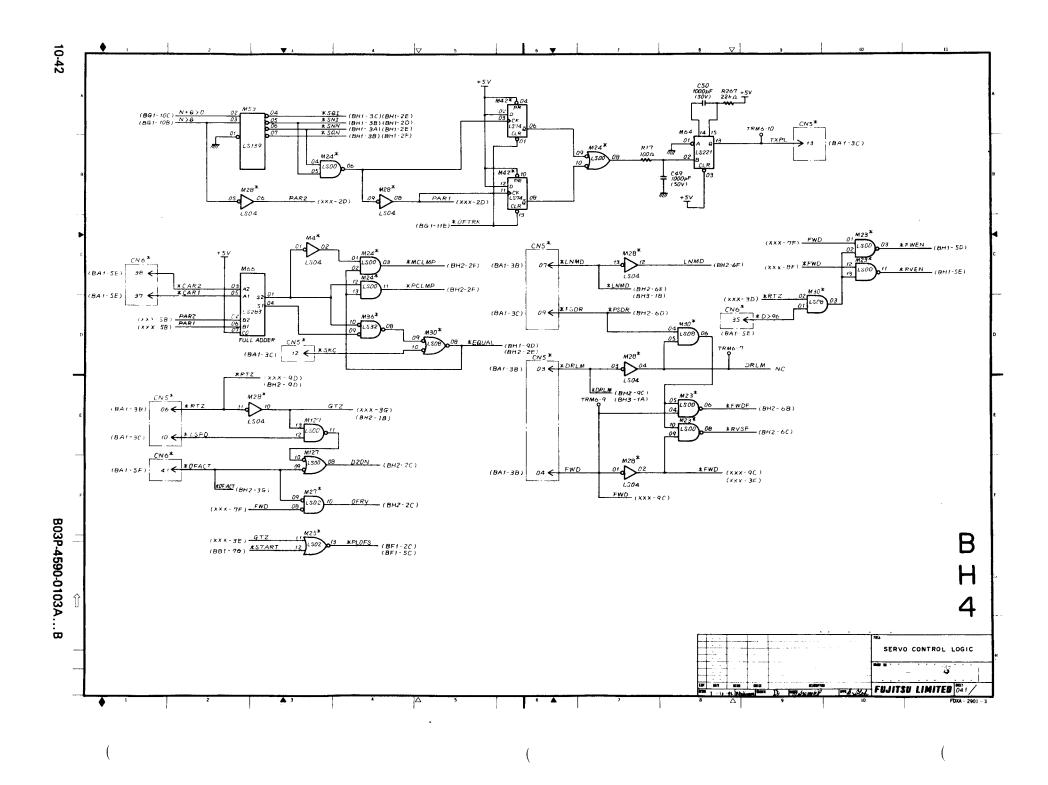


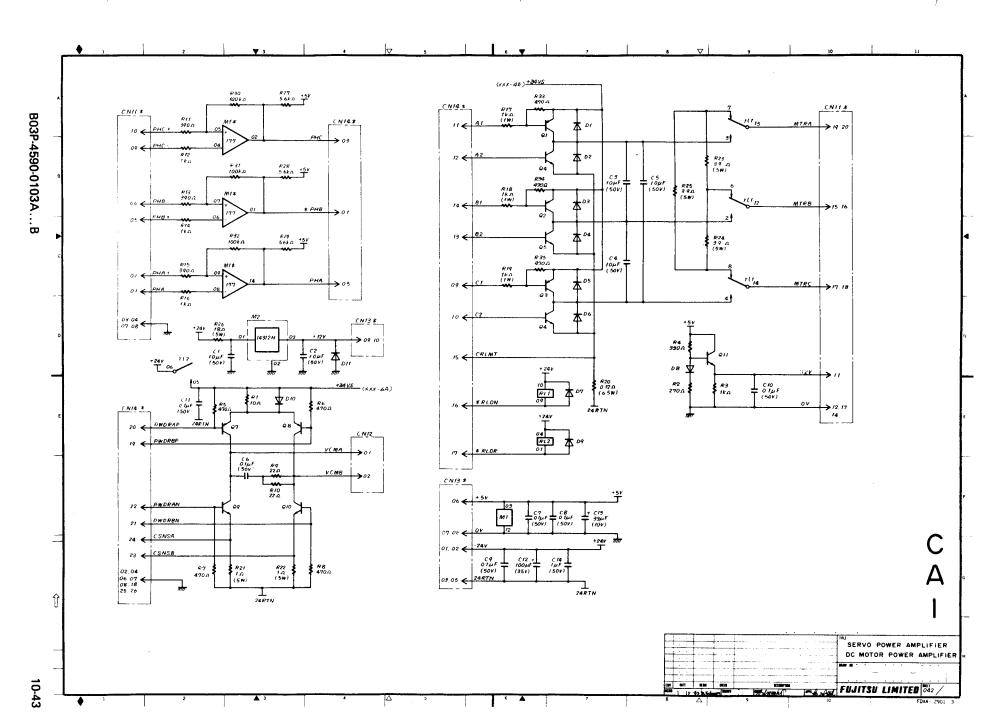


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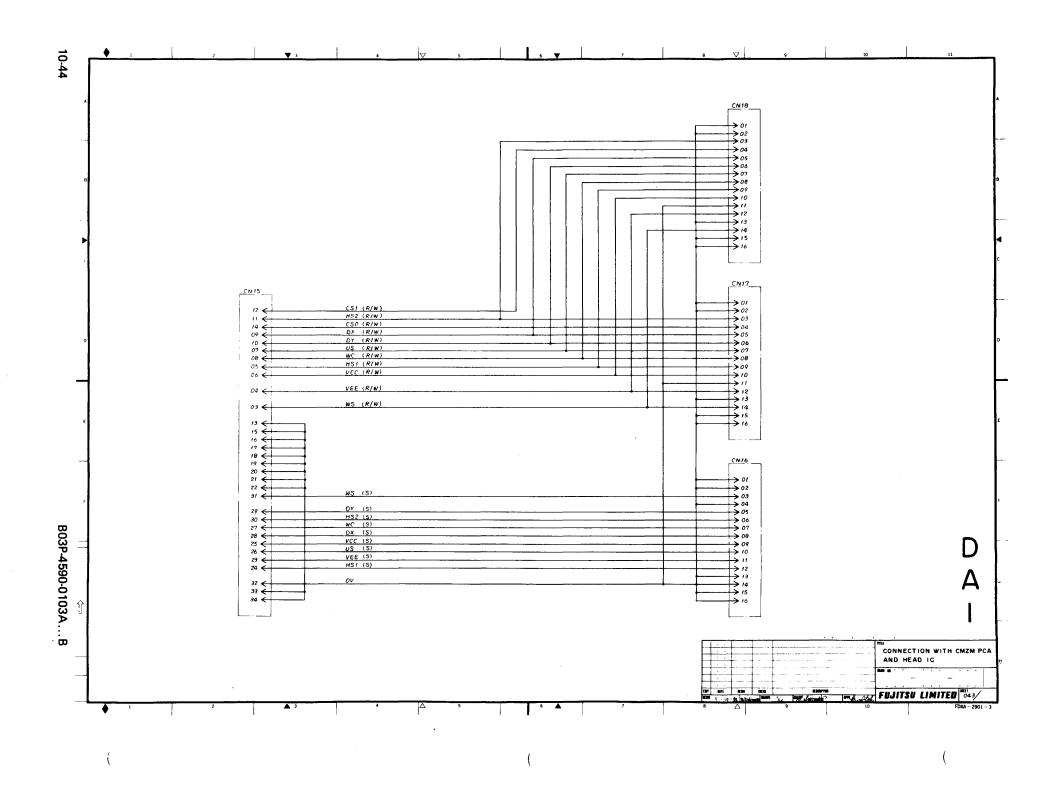


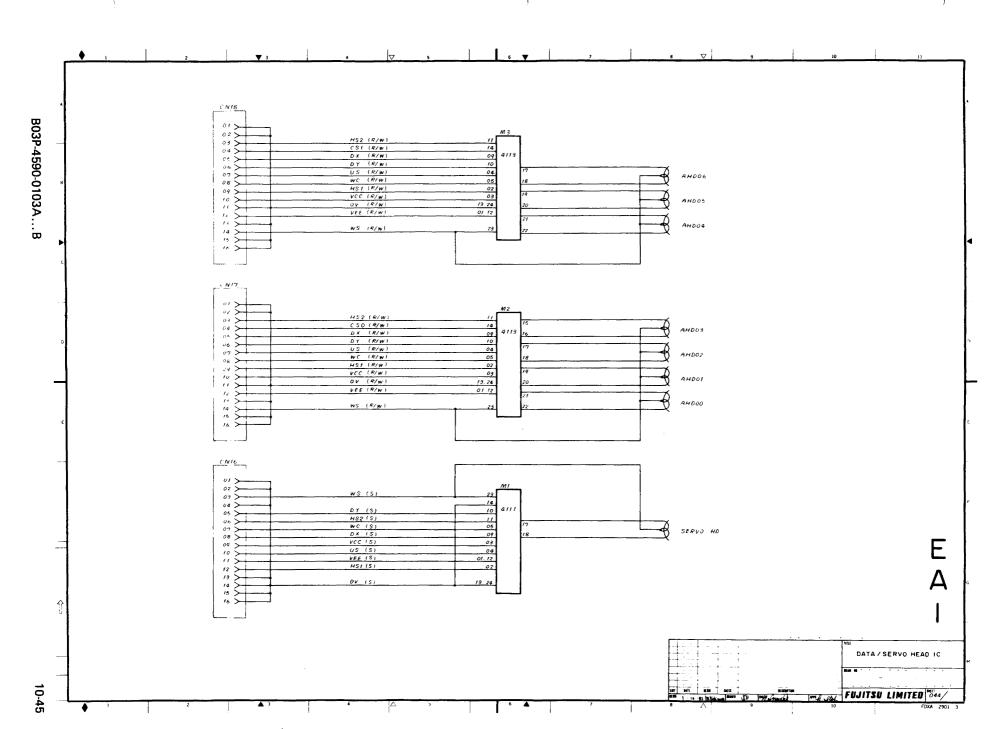


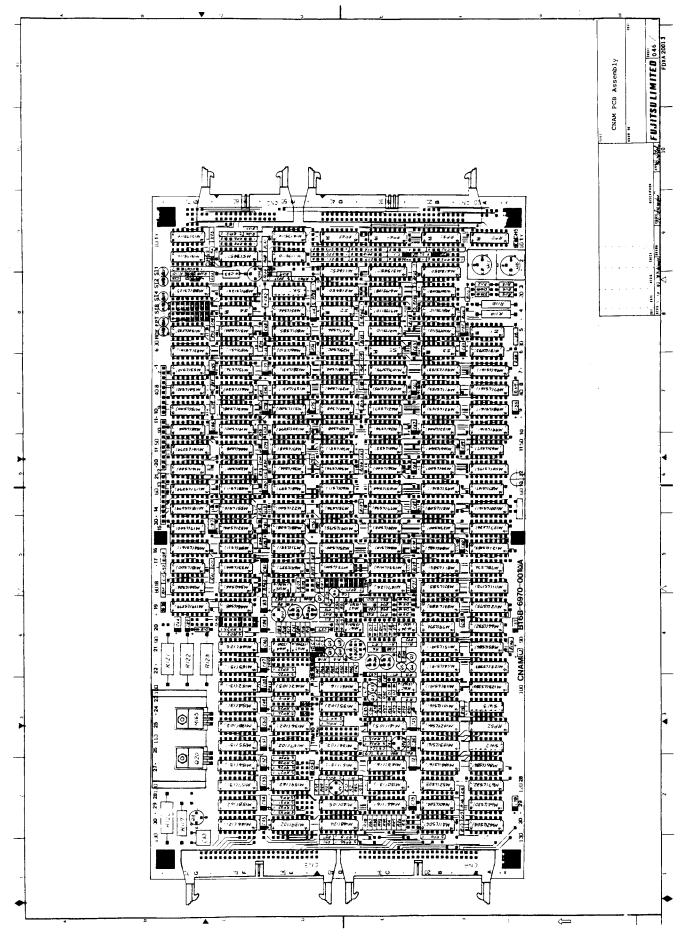


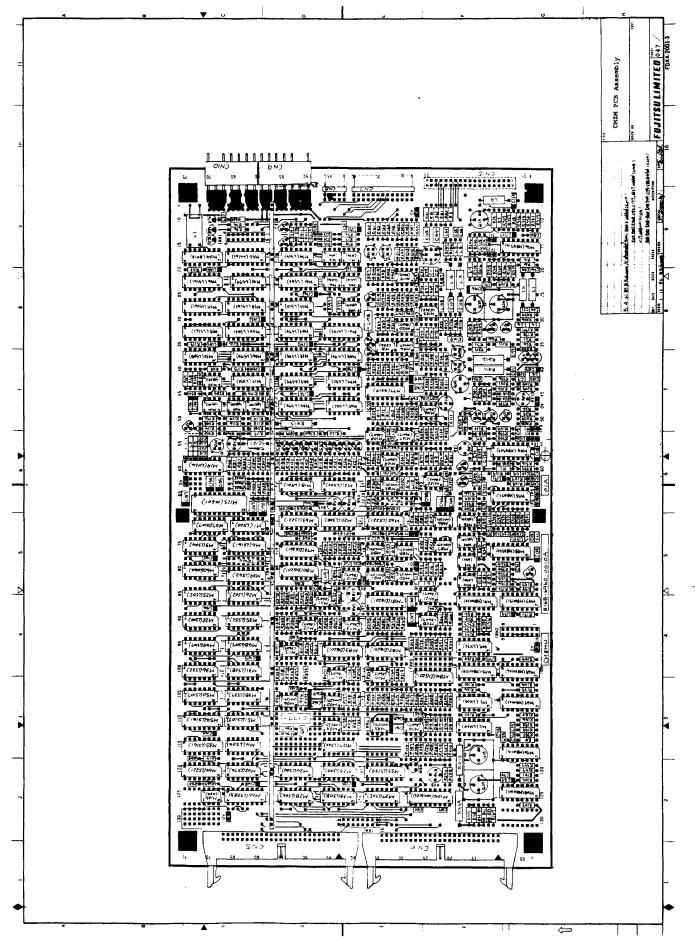


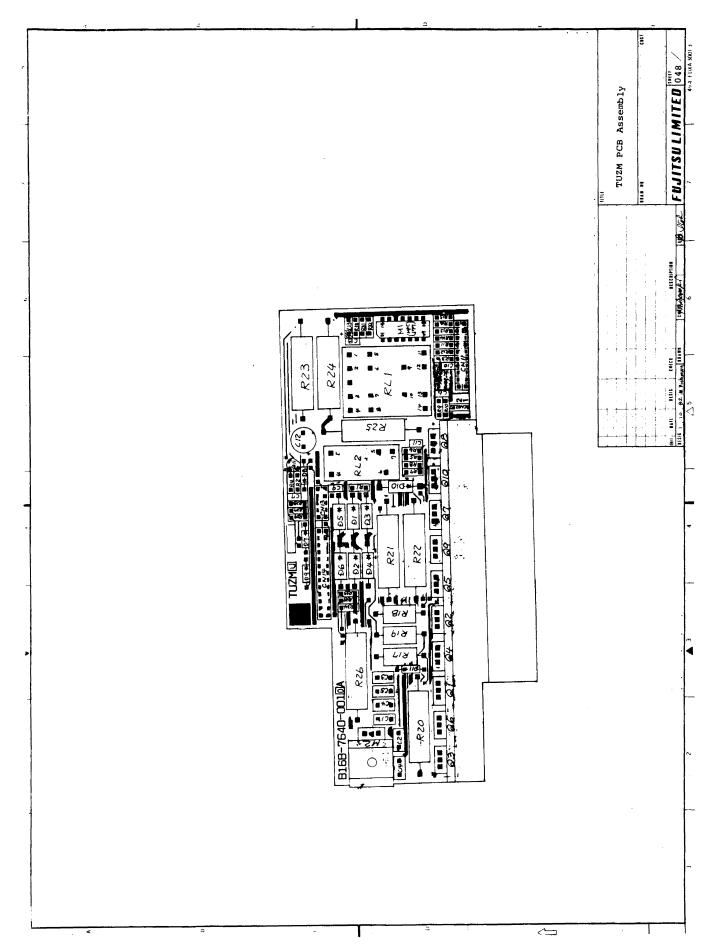
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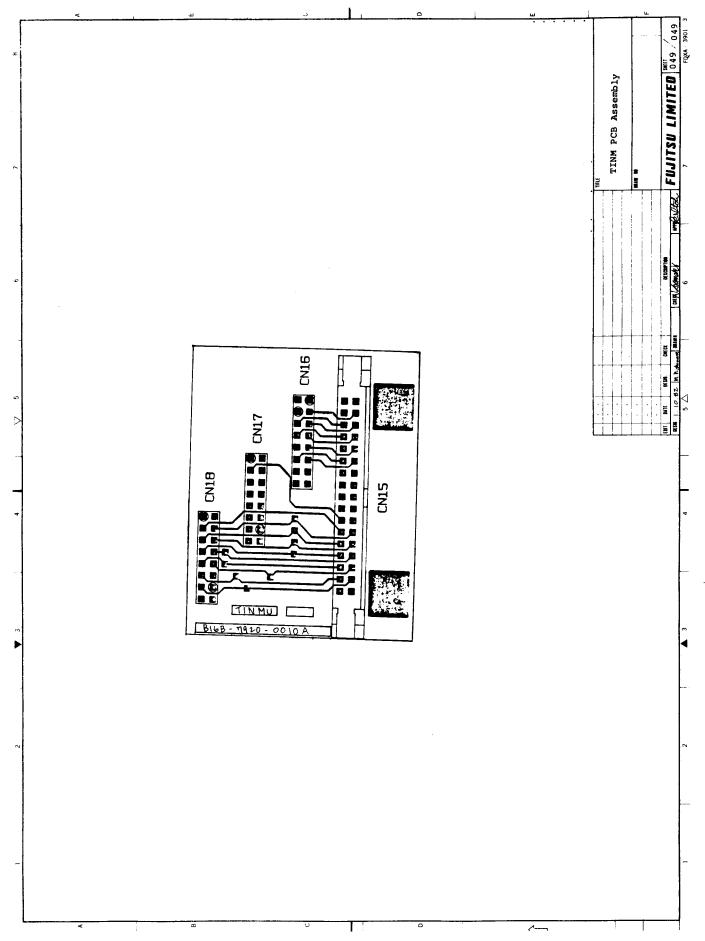












10.2 DUAL CHANNEL SCHEMATICS

This schematics is applied to the dual channel option.

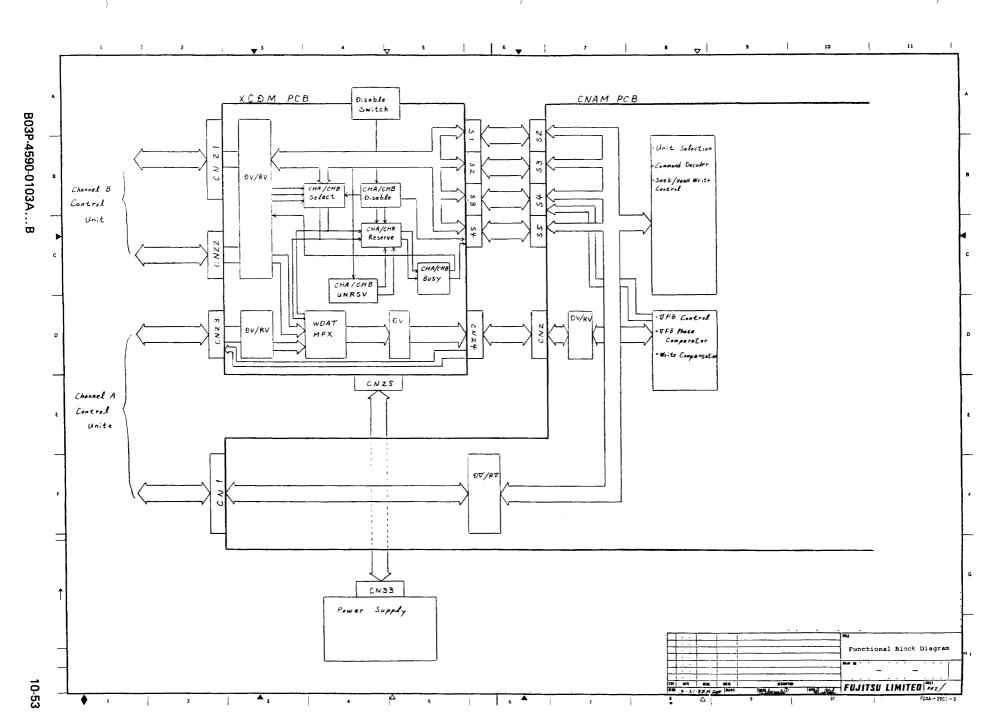
Therefore, dual channel option is installed to drives which machine revision is fram A7 up.

If the machine revision of drive is up to A6, dual channel option cannot be install to that drive without rework.

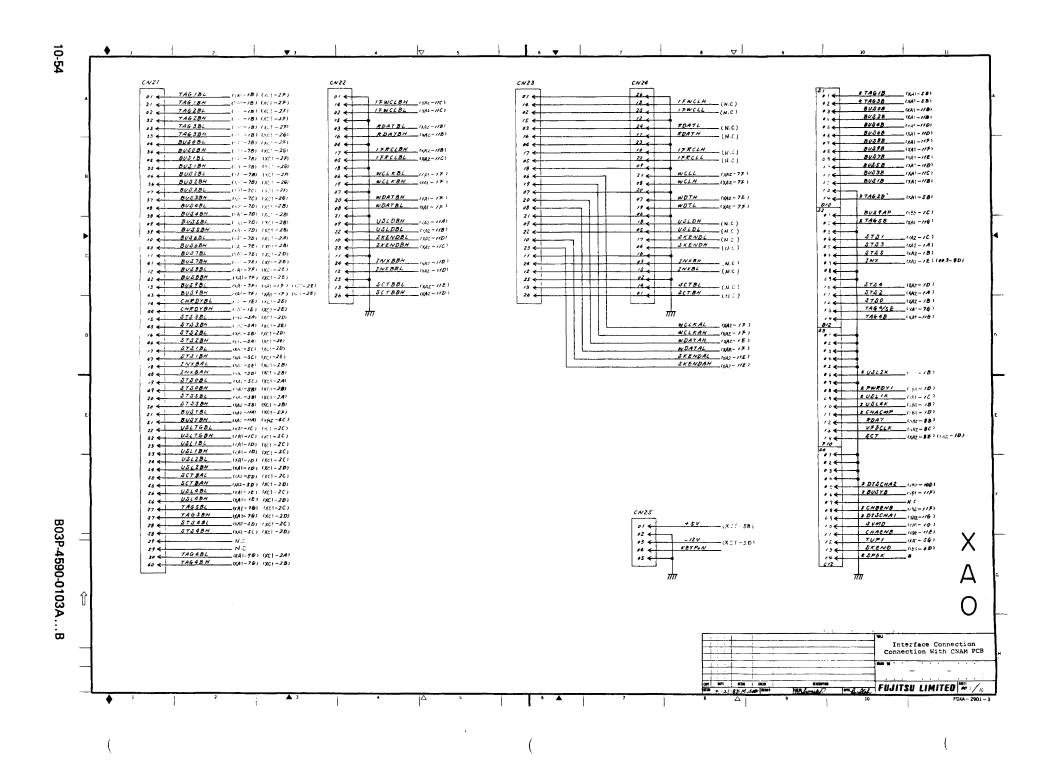
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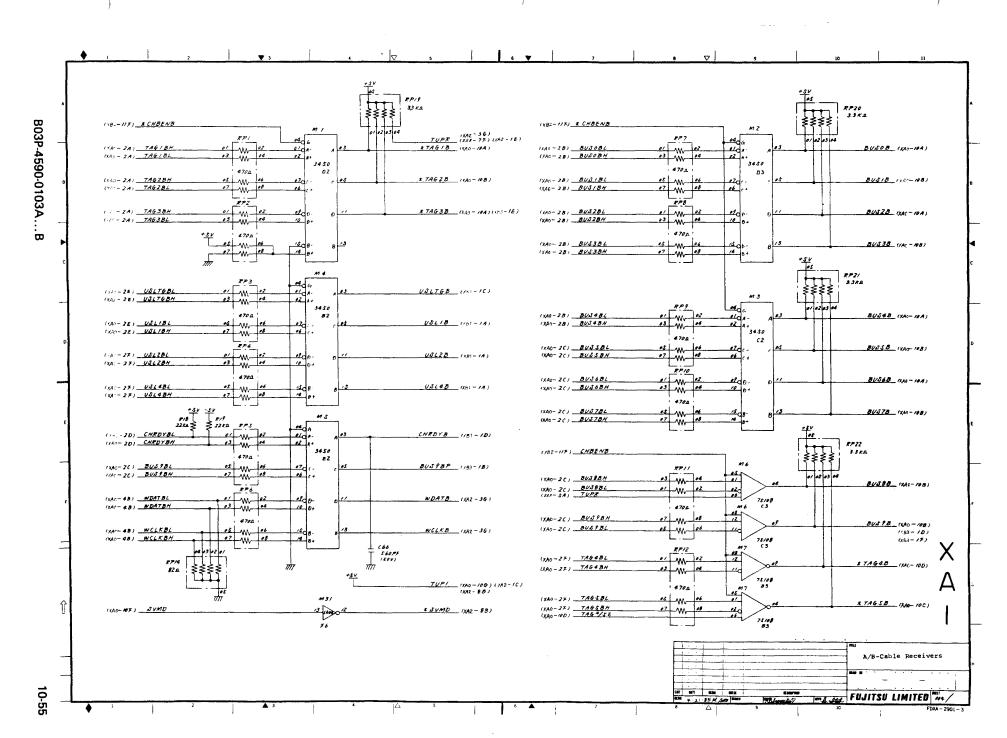
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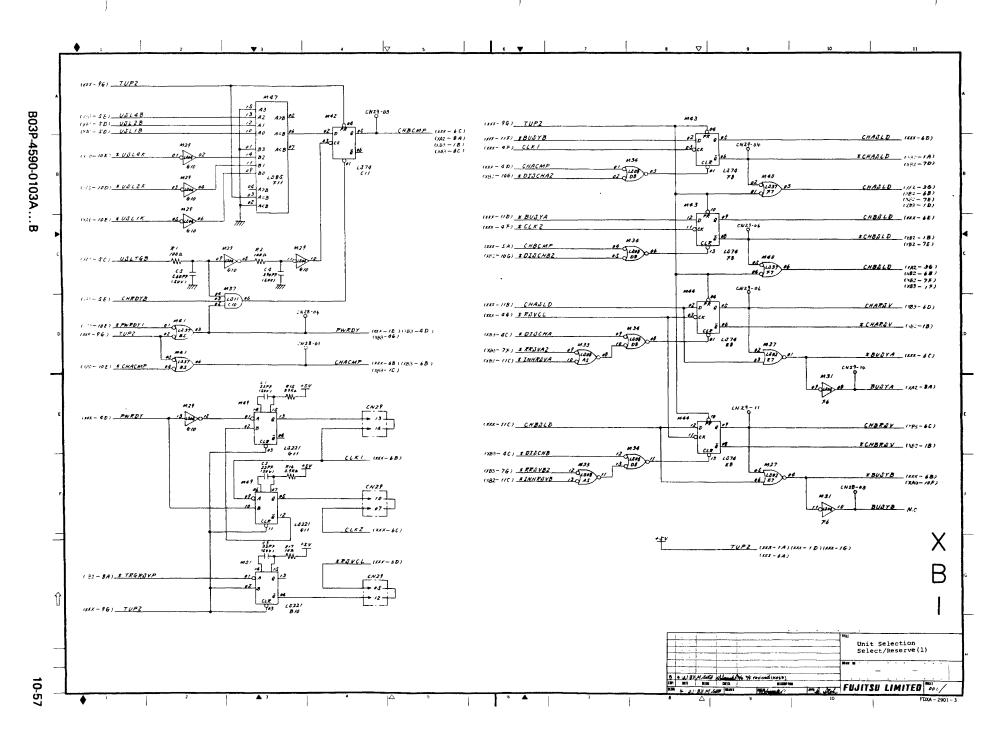
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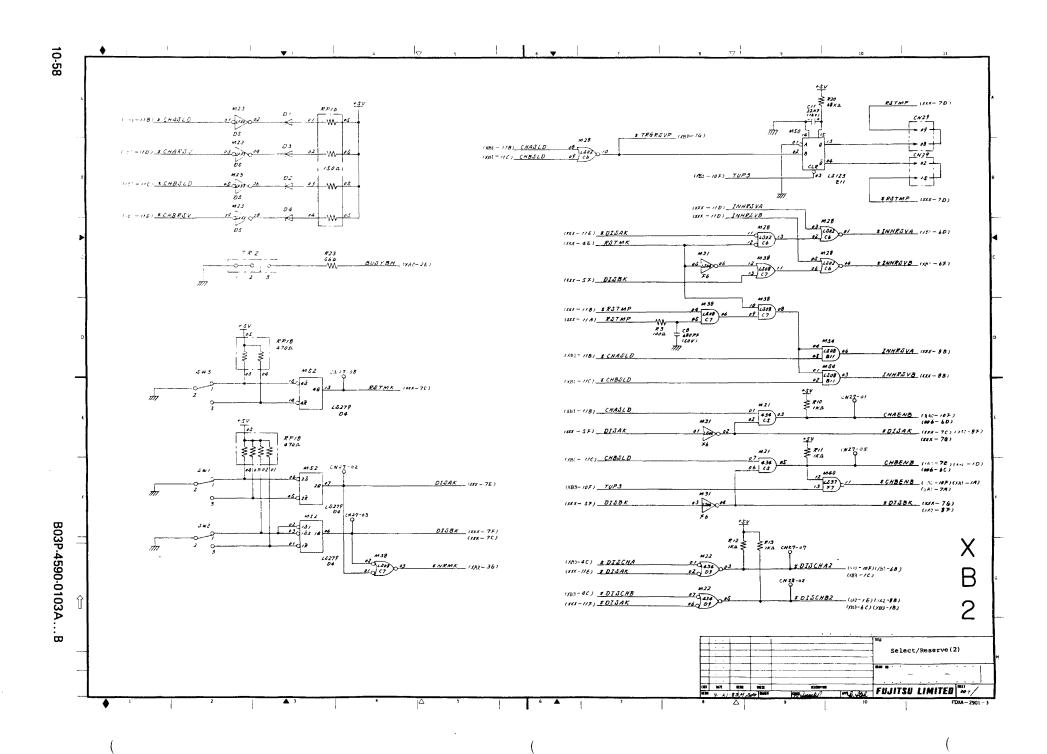


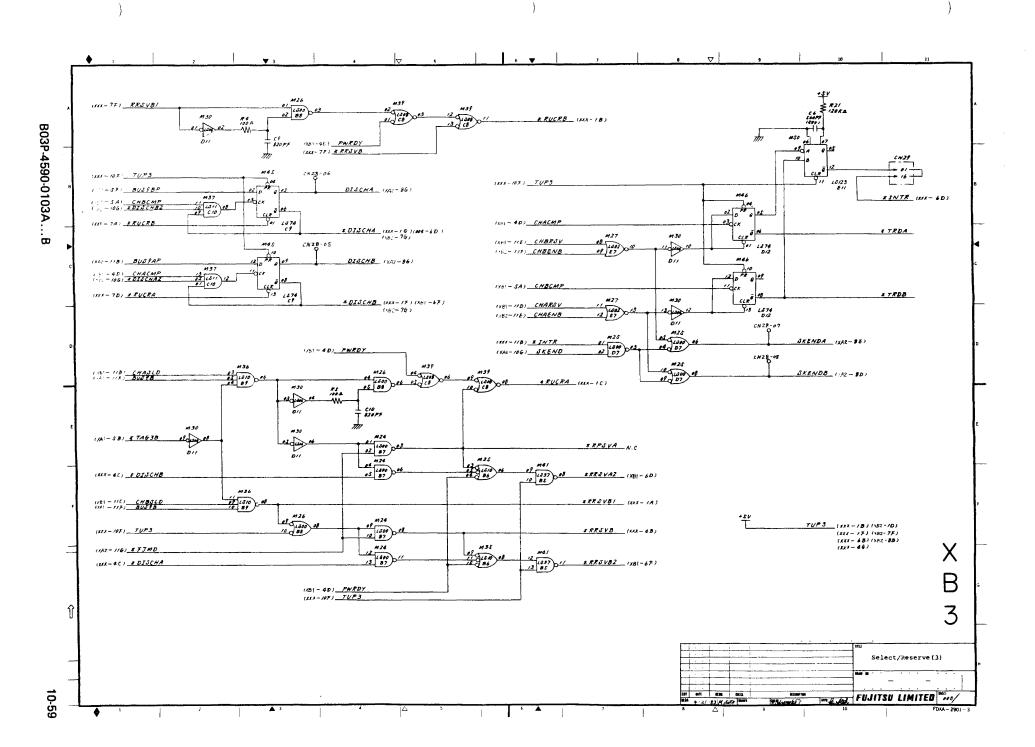
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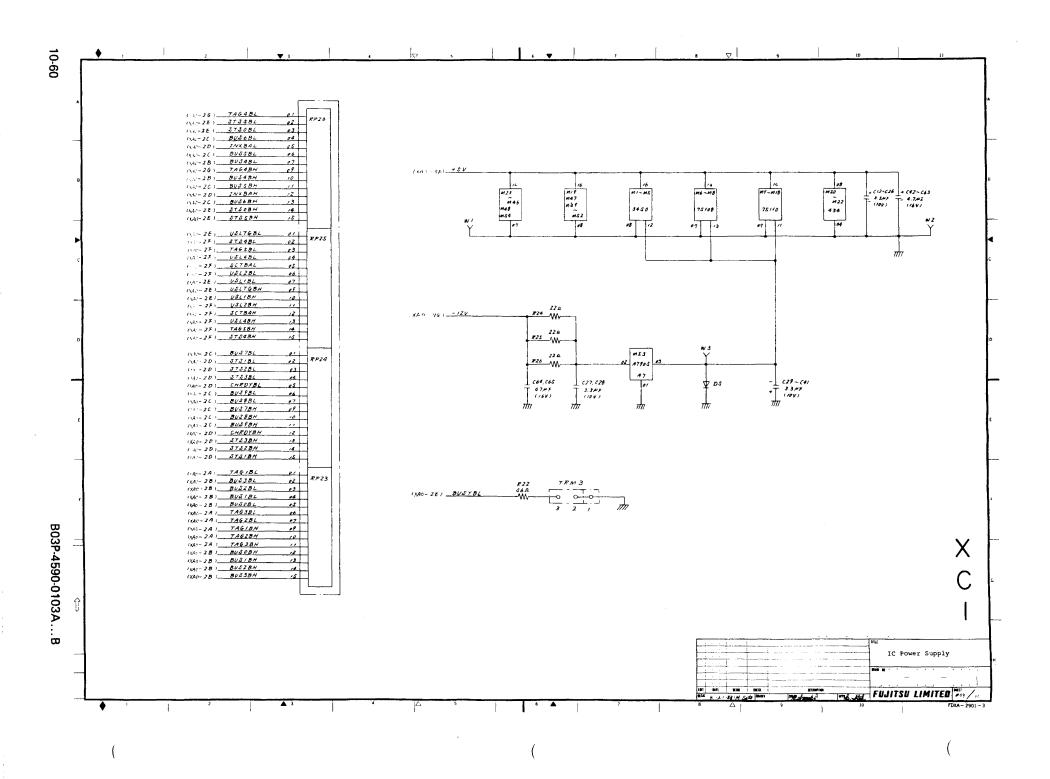


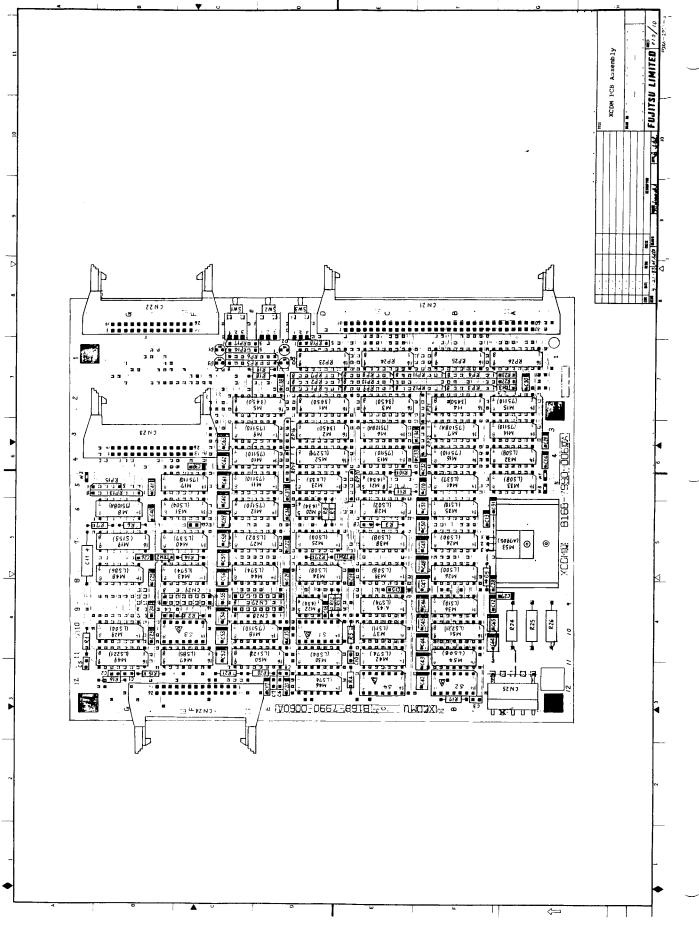












**** MEDIA DEFECT LIST ****

DATE: 83 0831 CUSTOMER: DE SERIAL NO:012934 SERIAL NO:12934 MODEL: B03B-4595-B002A NO CYLINDER HEAD POS/BYTES LEN/BITS SCT/ 64 PAGE- 1 1 0027(39) 00(0) 36B1(14001) 0003(3) 12 2 OODD(221) 03(3) 4139(16697) 006B(107) 4 3 OOF2(242) O1(1) OB73(2931) 0003(3) 1 4 OOF5(245) O3(3) 4DAS(19880) 0003(3) 1 02(2) 5 0150(348) 389C(14492) 0001(1) 1 0172(370) 01(1) 1 09BA(2490) 0002(2) 7 0172(370) 02(2) 2073(11379) 0005(5) 1 8 9 10 11 12